

ZSSC3281

Dual Channel Sensor Signal Conditioner IC for Resistive and Capacitive Sensors

The ZSSC3281 is a dual path sensor signal conditioning IC (SSC) for highly accurate amplification, digitization, and sensor-specific correction of sensor signals. The ZSSC3281 is suitable for resistive and capacitive sensors, as well as external voltage-source element and single-element sensors (for example, Pt100 and external temperature sensor diodes) powered by an on-chip current source. Digital compensation of the sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via a 32-bit ARM M3 based math core running a correction algorithm with calibration coefficients stored in a non-volatile, reprogrammable memory. The programmable, integrated sensor front-end allows optimally applying various sensors for a broad range of applications.

The ZSSC3281 provides measurement value readouts and programming capabilities via an I2C, SPI, or one-wire interface (OWI). Absolute and ratiometric voltage, current-loop, or interrupt outputs are supported by the ZSSC3281.

Applications

- Calibrated, continuously operating sensors with digital interface and/or analog output: (absolute or ratiometric) voltage or current loop output
- Enables smart, digital sensors for energy-efficient solutions
- (Dual/Diff.) pressure, flow and level sensing
- Industrial applications; for example, process/factory automation
- Consumer / white goods, for example, HVAC, weight scales
- Medical applications, for example, blood pressure, continuous smart health monitors

Features

- Digital communication and calibration interfaces:
 - SPI up to 12MHz
 - I2C (Standard, Fast, Fast+) and I3C SDR
 - One-wire-interface (OWI), up to 100kBit/s
- Accommodates nearly all resistive bridge sensor types (signal spans from 1mV/V up to 500mV/V)
- Supports different sensor element configurations:
 - Resistive bridge or half-bridge
 - Resistive divider string
 - Voltage source
- Accommodates nearly all capacitive sensor types
 - Single or dual capacitive cells
 - Isolated or grounded
 - Shield driver available
- On-chip temperature sensor
- External temperature sensing supported, for example, sensor-bridge as temperature detector, external diode, etc.
- Programmable 16-bit digital-to-analog-converter and output (supporting “True-0Volt”-output):
 - (0V to 1V) or (0V to 5V) absolute voltage output
 - VDD-ratiometric voltage output
 - 4mA to 20mA current-loop output supported
 - 0V to 10V absolute-voltage output supported
- Wide operational temperature and supply range
- On-chip voltage regulators for sensor supply, and IC operation item Support for extra regulation by external transistor, for example, JFET (especially for industrial supply voltages >5.5VDC)
- Programmable sensor-signal-conditioning math core
- Reprogrammable, nonvolatile memory (NVM)
- On-chip diagnostics:
 - Sensor connection
 - AFE self-test
 - Memory integrity

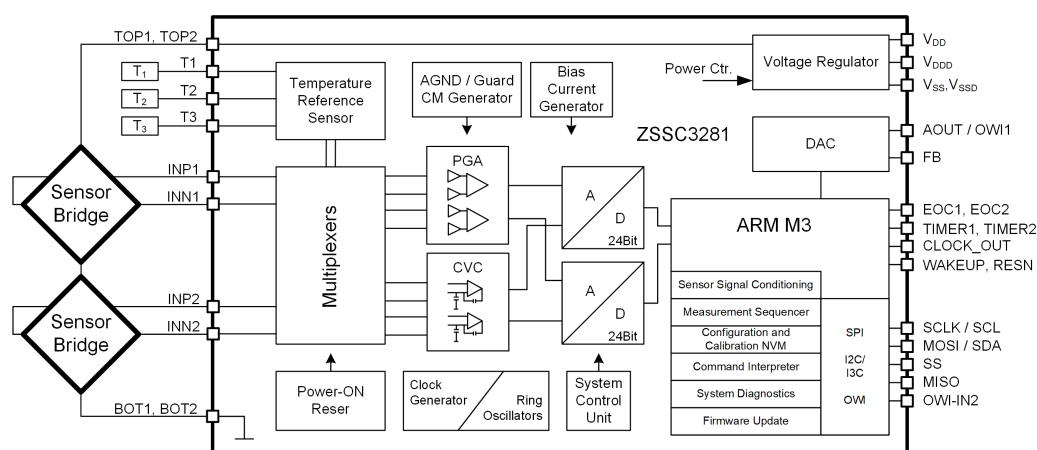


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1 Overview

1.1 Block Diagram

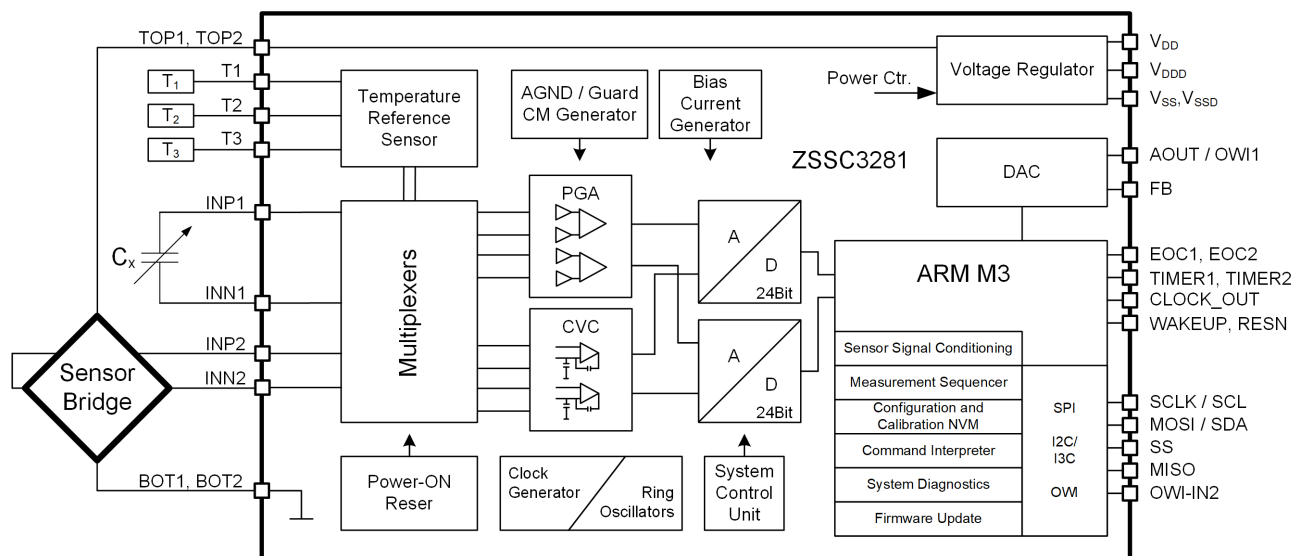


Figure 2: Block Diagram

1.2 Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
ZSSC3281CI1B	DICE on 304µm unsawn wafer no inking		Wafer Box	-40 to 125°C
ZSSC3281CI5B	DICE on 304µm unsawn wafer with inking		Wafer Box	-40 to 125°C
ZSSC3281CI5C	DICE on 304µm sawn on frame wafer with inking		Wafer Box	-40 to 125°C
ZSSC3281CI1D-ES	DICE on 304µm wafer no inking, only engineering samples		Waffel Pack	-40 to 125°C
ZSSC3281CI3R	5 x 5 mm2 NDG40S1 (40-VFQFPN)	MSL1	13 inch Reel	-40 to 125°C
ZSSC3281CI8R	5 x 5 mm2 WLCSP	MSL1	13 inch Reel	-40 to 125°C
ZSSC3281KIT	Modular ZSSC3281 SSC Evaluation Kit including three interconnecting boards, five ZSSC3281 VFPQFN samples, and cable. Software is available for download on www.renesas.com/ZSSC3281 .			

Note: All ZSSC3281 product options will be delivered with firmware version 1.5.0. An update of the firmware to 1.6.0 is possible and described in section 11.

1.3 Pin Configuration

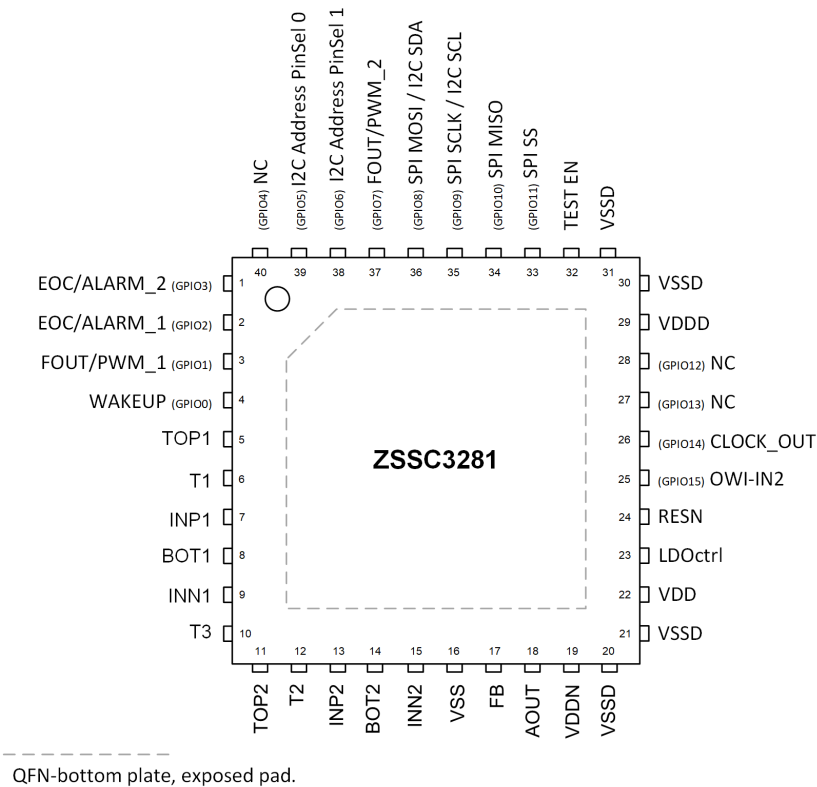


Figure 3: Pin Layout QFN40

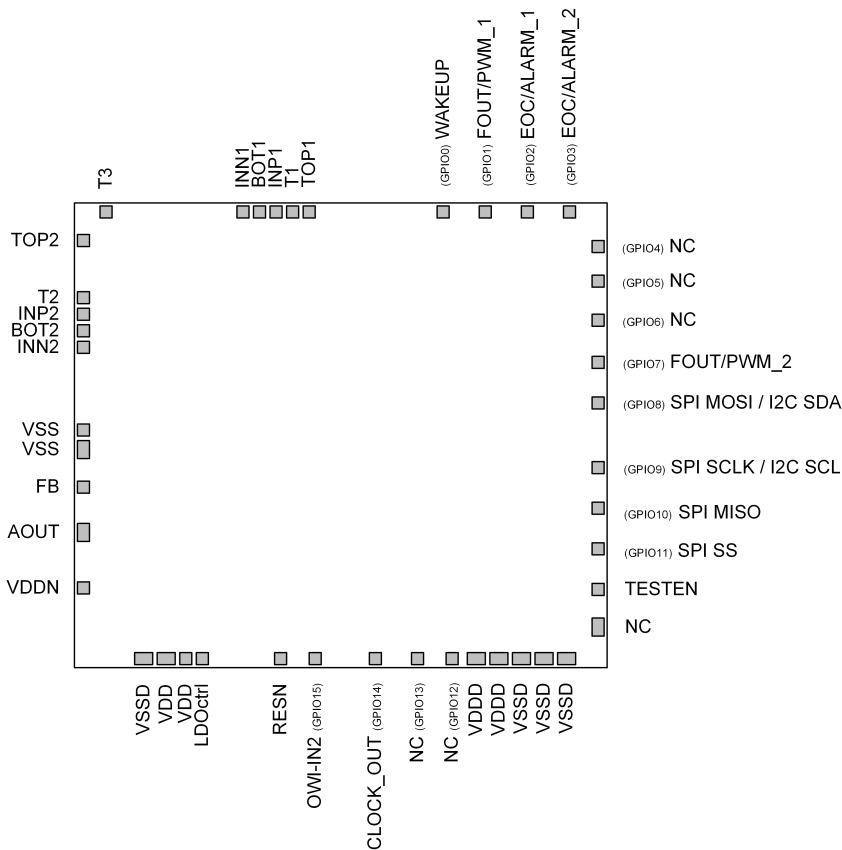


Figure 4: Pad Layout on Die

1.4 Pin Descriptions

QFN40 Pin Number	Name	Type	Description
1	EOC/ALARM_2	Digital Input/Output	GPIO3: mapped to EOC2 function
2	EOC/ALARM_1	Digital Input/Output	GPIO2: mapped to EOC1 function
3	PWM/FOUT_1	Digital Input/Output	GPIO1: mapped to TIMER2 function
4	WAKEUP	Digital Input/Output	GPIO0: mapped to WAKEUP function
5	TOP1	Analog Input/Output	Positive (resistive bridge 1) supply
6	T1	Analog Input/Output	External temperature sensor 1
7	INP1	Analog Input/Output	Positive (resistive bridge 1) signal or sensor signal input for Capacitive Frontend
8	BOT1	Analog Input/Output	Sensor (resistive bridge 1) ground
9	INN1	Analog Input/Output	Negative (resistive bridge 1) signal or sensor signal input for Capacitive Frontend
10	T3	Analog Input/Output	External temperature sensor 3 or Shield driver for capacitive frontend
11	TOP2	Analog Input/Output	Positive (resistive bridge 2) supply
12	T2	Analog Input/Output	External temperature sensor 2 or Shield driver for capacitive frontend
13	INP2	Analog Input/Output	Positive (resistive bridge 2) signal or sensor signal input for Capacitive Frontend
14	BOT2	Analog Input/Output	Sensor (resistive bridge 2) ground
15	INN2	Analog Input/Output	Negative (resistive bridge 2) signal or sensor signal input for Capacitive Frontend
16	VSS	Ground	Power supply ground
17	FB	Analog Output	Current-loop application feedback output (level below VSS). No connection if not used.
18	AOUT/OWI	Analog Output Digital Input/Output	Analog smart-sensor output signal and/or OWI interface input/output line.
19	VDDN	Analog Output	Negative voltage output, charge pump buffer cap
20	VSSD	Ground	Digital power supply ground
21	VSSD	Ground	Digital power supply ground
22	VDD	Supply	Power supply
23	LDOctrl	Analog Output	Control output (reference signal) for (optional) external regulator / supply control loop
24	RESN	Digital Input	Digital IC reset (low active); internal pull-up
25	OWI-IN2	Digital Input/Output	GPIO15: mapped to OWI-IN2 function
26	CLOCK_OUT	Digital Input/Output	GPIO14: mapped to CLOCK_OUT function
27	N.C.	Digital Input/Output	GPIO13: Renesas internal use only. Debug interface
28	N.C.	Digital Input/Output	GPIO12: Renesas internal use only. Debug interface
29	VDDD	analog I/O	Buffer cap connection for internal VDDD
30	VSSD	Ground	Digital power supply ground
31	VSSD	Ground	Digital power supply ground
32	TESTEN	–	Renesas internal use only. Connect to VSSD
33	SPI SS	Digital Input/Output	GPIO11: mapped to SPI SS
34	SPI MISO	Digital Input/Output	GPIO10: mapped to SPI MISO
35	SPI SCLK / I2C SCL	Digital Input/Output	GPIO9: mapped to SPI SCLK / I2C SCL
36	SPI MOSI / I2C SDA	Digital Input/Output	GPIO8: mapped to SPI MOSI / I2C SDA
37	PWM/FOUT_2	Digital Input/Output	GPIO7: mapped to TIMER 1
38	I2C Address PinSel 1	Digital Input/Output	GPIO6: mapped to I2C Address PinSel 1
39	I2C Address PinSel 0	Digital Input/Output	GPIO5: mapped to I2C Address PinSel 1
40	N.C.	Digital Input/Output	GPIO4: not mapped
	Exposed PAD	-	QFN-bottom plate, Die-bottom/substrate. Connect to VSS, PAD connection used for heat dissipation and enhanced EMC robustness.

2 Specifications

2.1 Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
T _J	Junction temperature			135	°C
T _S	Storage temperature		-45	150	°C
	ESD: Human Body Model Tested per JS-001-2017	Pins: INPx, INNx, TOPx, BOTx, Tx, VDDD		2000	V
		Pins: GPIOx, VDD, VDDN, VSS, VSSD, LDOctrl, AOUT/OWI, FB, RESN, NC		4000	V
	ESD: Charged Device Model Tested per JS-002-2014	All Pins		750	V
	Latch-up	Tested per JESD78E; Class 2, Level A	-100	+100	mA
V _{DD_max}	Maximum allowed for voltage supply	Referenced to VSS	-0.3	6.5	V
V _{IF_max}	Voltage at digital I/O	Referenced to VSSD	-0.3	5.5	V
V _{FB_max}	Voltage at FB pin	2-wire Current Loop Mode	-2	2	V

WARNING: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Symbol	Parameter	Conditions	Typical	Units
θ_{JA}	Theta JA	40Ld 5×5 QFN Package, 0 m/s air flow	25.8	°C/W
		40Ld 5×5 QFN Package, 1 m/s air flow	22.4	°C/W
		40Ld 5×5 QFN Package, 2 m/s air flow	20.8	°C/W
θ_{JB}	Theta JB	40Ld 5×5 QFN Package	1.3	°C/W
θ_{JC}	Theta JC	40Ld 5×5 QFN Package	24.4	°C/W

2.3 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V _{DD}	Power supply voltage	1.8			
	Flash write/erase	2.7		5.5	V
	With optional "True-0V" at analog output	2.7			
T _J	Junction temperature (depending on the ordered device, see subsection 1.2 for details.)	-40		125	°C
C _{VDD}	External capacitance between VDD and VSS, without external supply transistor regulation	10 -20%		22 +20%	μF
	External capacitance between VDD and VSS, with (optional) external supply transistor regulation	10 -20%		10 +20%	
C _{V3D}	External capacitance between VDDD and VSS	1 -20%		1 +20%	μF
C _{VDDN}	External capacitance between VDDN and VSS, with optional "True-0V" at analog output	1 -20%		1 +20%	μF
C _{TOP_EMC}	Recommended, external capacitance between TOP and VSS for electro-magnetic immunity (EMI)	0	6.8	8	nF
C _{AOUT_EMC}	Recommended, external capacitance between AOUT versus VDD and VSS for EMI suppression ¹	0	22	33	nF
I _{Sensor}	Load current through external sensor element ²	0.005	0.5	2	mA
V _{DioDrop}	External temperature diode and RTD input range, drop over external element referenced to T1, T2, T3 pin	0.2		1.2	V
V _{Sens_in}	Absolute sensor signal input level, INN, INP pins	0.2		1.2	V
I _{max_AOUT_V}	Maximum current load at AOUT pin for voltage outputs	0	5		mA
S _{RVDD_POR}	Recommended VDD rise slew rate for power-on-reset (POR)	1.5			V/ms
I _{max_GPIO}	Maximum overall GPIO driver strength			120	mA

¹ For applications with OWI interface or analog voltage-output.

² With ratiometric sensor supply configuration, for example, a ratiometric bridge or bridge as temperature sensor with internal or external temperature sensitive resistor

2.4 Electrical Specifications

All parameter values are valid only under operating conditions specified in subsection 2.3 All voltages are referenced to VSS.

Table 1: IC Supply

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{IC}	Current consumption, active mode: • low power (current loop)	Excluding connected sensor elements (external LDO enabled)		3.3	3.5	mA
	• high power (depending on settings)			8	15	
$V_{DD,LDO}$	VDD generated with external depletion NMOS	Programmable in 4 steps: • 3V	2.85	3	3.15	V
		• 4V	3.80	4	4.20	
		• 5V	4.75	5	5.25	
		• 5.25V	5.00	5.25	5.50	
VDDA	Internally generated analog supply		1.6	1.65	1.85	V

Table 2: Sensor Supply

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
TOP	Sensor bias voltage in ratiometric supply mode	Ratiometric sensor voltage supply		VDDA		V
I_{bias_TOP}	Sensor bias current used in Source Mode	Programmable in 10 steps: 0μA, 5μA, 10μA, 20μA, 40μA, 80μA, 100μA, 160μA, 200μA, 500μA	0		500	μA
I_{biasN_BOT}	Sensor current used in sink mode	Programmable in 2 steps: 20μA, 100μA	20		100	μA
I_{ERR}	Relative bias current (I_{bias_TOP} and I_{biasN_BOT}) error	Overall	-10		10	%
		Over-temperature	-1		1	
R_{TH}, R_{TL}	TOP/BOT bias resistor	Programmable in 12 steps: open, 1.33kΩ, 2kΩ, 4kΩ, 8kΩ, 10kΩ, 14kΩ, 18kΩ, 20kΩ, 24kΩ, 28kΩ, 40kΩ	1.3		40	kΩ
dR_{TH}, dR_{TL}	TOP/BOT bias resistor process variation		-30		30	%
TK of R_{TH}, R_{TL}	TOP/BOT bias resistor temperature variation	T = -55°C to 125°C			1.3	%

Table 3: Analog-to-Digital Converter (ADC, A2D)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
r_{ADC}	Resolution		10	16	24	Bit
V_{ADCmid} (AGND)	Differential ADC input Common Mode	With internal regulator supplying TOP pin, typical: $V_{TOP}/2 = 875mV$ (=PGA output Common Mode level)		0.5		V_{TOP}
$\Delta_{ADC,c}$	Differential input offset shift	Sensor signal offset versus maximum sensor signal. Programmable in 8 steps.	0		7/8	V_{shift}/V_{fs}
ENOB ¹	Effective number of bits, $3\sigma_{Noise}$ based	Gain = 1.32, $r_{ADC} = 24$ bit, no oversampling		17		Bit
		Gain = 28, $r_{ADC} = 16$ bit, no oversampling		12		Bit
		Gain = 495, $r_{ADC} = 24$ bit, no oversampling		11		Bit

¹ $ENOB = LOG_2 \left(\frac{2^{r_{ADC}}}{3\sigma_{Noise}} \right)$ with for example, r_{ADC} [Bit] = 24.

Table 4: Digital-to-Analog Converter (DAC) and Analog Output

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
VDD	VDD operating range	AOUT modes using 1V buffer	1.8		5.5	V
		AOUT modes using VDD buffer	2.7		5.5	
$t_{AOUTsettle}$	Time between digital value applied at DAC and voltage at VOUT	10% to 90% input step: V_{AOUT} at 90% of final value			100	μs
V_{OUT_START}	Voltage at AOUT during startup			0		V
V_{AOUT}	Output voltage at pin AOUT	Ratiometric Voltage Mode (VDD Buffer)	0		VDD	V
		1V absolute Voltage Mode (1V Buffer)	0		1	
		3V absolute Voltage Mode (VDD Buffer)	0		3.1 ¹	
		5V absolute Voltage Mode (VDD Buffer)	0		5 ²	
		10V absolute Voltage Mode (VDD Buffer)	0		5 ²	
I_{OUTMAX}	Short current limit at pin AOUT	AOUT modes using VDD Buffer Short to VDD or VSS Programmable in 4 steps	3	5	9	mA
			8	12	20	
			13	19	25	
			18	25	32	
C_{load}	Load capacitance at AOUT	2-Wire Current Loop Mode			2	nF
		All other modes (for example, cap for EMC: 33nF, ECU load: 10nF)	10 ³		50	
r_{DAC}	Resolution			16		Bit

¹ VDD must be $\geq 3.5V$

² VDD must be $\geq 5.25V$

³ If Power-Ground Loss detection is enabled, ensure a minimum of 10nF capacitance is connected to AOUT.

Table 5: Programmable-Gain Amplifier (PGA)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
G_{amp}	Gain	120 steps	1.32		495	V/V
G_{err}	Gain error	Referenced to nominal gain: Gain = 1.32 to 5	-2.5	0	-2.5	%
		Gain = 6 to 125	-5		5	
		Gain = 126 to 495	-10		10	
$G_{errTemp}$	Gain error over-temperature	Sensors with temperature compensation do not require calibration over varying temperature ranges.	-0.2		0.2	%
V_{CMin}	Supported input Common Mode		0.2	0.5	0.7	V_{TOP}
V_{ioffsc}	Differential input offset shift	Programmable in 30 steps: Gain1 ≤ 223	-28.1	0	28.1	mV
		Gain1 = 275	-22.5	0	22.5	

Table 6: Sensor Signal Conditioning (SSC) Performance for Resistive Sensor

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{SSCout}	Output (update) rate	<ul style="list-style-type: none"> 3 measurements: signal+, signal-, diagnosis $r_{ADC} = 16\text{bit}$ SSC-corrected digital output 		1.3		kHz
		<ul style="list-style-type: none"> 3 measurements: signal+, signal-, diagnosis $r_{ADC} = 14\text{bit}$ SSC-corrected digital output 		2.245		kHz
		<ul style="list-style-type: none"> 2 measurements: signal+, diagnosis $r_{ADC} = 14\text{bit}$ SSC-corrected digital output 		3.36		kHz
$t_{stepresp}$	Step response	<ul style="list-style-type: none"> 3 measurements: signal+, signal-, diagnosis $r_{ADC} = 16\text{bit}$ SSC-corrected digital output 		1.38		ms
		<ul style="list-style-type: none"> 3 measurements: signal+, signal-, diagnosis $r_{ADC} = 14\text{bit}$ SSC-corrected digital output 		0.84		ms

Table 7: Analog Inputs for Resistive Sensor

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{INP1} , V_{INN1} , V_{INP2} , V_{INN2}	Absolute sensor input	Voltages at INPx and INNx pin; resulting minimum/maximum differential voltages: $-800\text{mV} < V_{INDiff} < 800\text{mV}$	0.2		1.2	V
V_{TEXT}	External temperature diode or RTD input range	At T1, T2, T3 pin (see Table 2 and ExtTempBrdgIBias for available configuration options)	0.3		1.2	V
R_{SENSOR}	External sensor (bridge) resistance	TOP = 1.65V	0.825		60	k Ω
		2-wire Current Loop Mode	3.3		60	k Ω
$ V_{DIFFin} $	Differential input signal range	Referenced to sensor supply ($V_{DDA_{int}}$)			800	mV

Table 8: Diagnostics for Resistive Sensor

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_{open}	Broken sensor: values $>R_{open}$ set a failure flag	<ul style="list-style-type: none"> • INP1 vs. INN1 • INP2 vs. INN2 Note: INN is drawn to VSS! This is not applicable in sensor configuration with one bridge at both frontends!	100	120	150	k Ω
R_{short}	Shorted sensor: values $<R_{short}$ set a failure flag	<ul style="list-style-type: none"> • INP1 vs. INN1 • INP2 vs. INN2 • INP1 vs. INP2 • INP2 vs. INN1 	120		220	Ω
V_{drift}	AFE gain check, run measurement with dedicated gain, compare with stored values	Input value from RDAC is applied				
V_{RDAC}	RDAC differential output voltage	VDDAx = 1.65V: • S = 00		2		mV
		• S = 01		10		
		• S = 10		100		
		• S = 11		200		
R_{T_OPEN}	T1, T2, T3 connection check: open	Broken Tx sensor: values $>R_{T_OPEN}$ set a failure flag and can be configured in 3 level Note: INN is drawn to VSS! This is not applicable in sensor configuration with one bridge at both frontends!	1.6	2	3	M Ω
			0.4	0.5	0.6	
			0.07	0.1	0.13	
t_{T_OPEN}	Diagnosis time; depends on C_{IS} and R_{T_OPEN}	Time from diagnose enable to valid output	0.1		10	ms
R_{T_SHORT}	T1, T2, T3 connection check: short to TOP, BOT, INP, INN	Shorted Tx sensor: values $<R_{T_SHORT}$ set a failure flag: • configuration for Pt1000	320	500	650	Ω
V_{DDD_BOD}	VDDD brown out detection	$V_{DDD} < V_{DDD_BOD}$ set a failure flag	85	90	92	%VDDD
V_{LOSS}	Power/ground loss with respect to AOUT	<ul style="list-style-type: none"> • $V_{AOUT} - V_{DD} > V_{LOSS}$ • $V_{AOUT} - V_{SS} < V_{LOSS}$ 		0.2		V

Table 9: Power-Up

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t_{STA1}	Startup time	VDD ramp up to interface communication		7.5	10	ms
t_{STA2}		VDD ramp up to analog operation; depends on the configuration used		7.5	10	ms
t_{WUP1}	Wake-up time	Sleep to Active State interface communication		7.5	10	ms

Table 10: Oscillator

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{CLK_HF}	Internal HF-oscillator frequency	At $T=27^{\circ}\text{C}$	15.8	16	16.2	MHz
		Across temperature range	15		17	
f_{CLK_LF}	Internal LF-oscillator frequency		25	32	41	kHz

Table 11: Internal Temperature Sensor

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
Γ_{Temp}	Internal temperature sensor resolution	Differential output voltage		220		$\mu\text{V/K}$

Table 12: Digital IO Pins

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Input low voltage	voltage level where the input is recognized as low level			30	% VDD
V_{IH}	Input high voltage	voltage level where the input is recognized as high level	70			% VDD
V_{Ihys}	Input hysteresis		10		35	% VDD
V_{OL}	Output low voltage				8	% VDD
V_{OH}	Output high voltage		92			% VDD
I_{OL}	Output drive low current	$V_{PAD} = V_{OL}$: $VDD = 1.8V$	1		2.4	mA
		$VDD = 2.6V$	2.7		6.6	
		$VDD = 5V$	9		20	
I_{OH}	Output drive high current	$V_{PAD} = V_{OH}$: $VDD = 1.8V$	1.2		2.3	mA
		$VDD = 2.6V$	3.2		6.4	
		$VDD = 5V$	10.9		20.2	
I_{pullup}	Weak pull-up current at pin RESN	$V_{PAD} = 0V$: $VDD = 1.8V$	5		13	μA
		$VDD = 2.6V$	17		50	
		$VDD = 5V$	84		250	
$I_{pulldown}$	Weak pull-down current at pin WAKEUP	$V_{PAD} = VDD$: $VDD = 1.8V$	5		11	μA
		$VDD = 2.6V$	17		35	
		$VDD = 5V$	80		160	

Table 13: Serial Interfaces

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$f_{C,SPI}$	SPI clock frequency				12	MHz
$f_{C,I2C}$	I2C clock frequency				1	MHz
$f_{C,I3C}$	I3C clock frequency				12	MHz
C_{DOWI}	OWI data rate		0.25		100	kBit/s

Table 14: Flash Memory

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t_{PROG}	NVM program time	Programming time for complete configuration and calibration page: $f_{CLK_HF} = 16MHz$		360		ms
		$f_{CLK_HF} = 1MHz$	-	740	-	
n_{NVM}	NVM endurance	Number of reprogramming cycles	20000			Numeric
$t_{RET,NVM}$	Data retention		10			Years

3 Basic System Configuration

3.1 System Modes/System Start

The ZSSC3281 can operate in three different main operating modes:

Cyclic Mode	This is the default mode for continuously operating sensors. In this mode autonomous, cyclically repeated sensor measurements are performed and related digital and/or analog output updates are provided. The cyclic sequences for sensor measurements and system diagnostic measurements are configurable and allow to define the output update rate of the conditioned sensor signals. Cyclic Mode supports only a subset of the defined serial interface commands to guarantee deterministic input-output behavior (especially latencies) and to prevent accidental interruption of the conditioned sensor data stream.
Command Mode	This is the most appropriate mode for evaluation, test, and calibration purposes. In this mode, all supported serial interface commands are available. Command Mode can be used for applications requiring re-occurring digital interaction on functions that are not available in Cyclic Mode or certain system configuration changes.
Sleep Mode	This is the default mode for non-continuously operating sensors. In this mode WAKEUP (GPIO0) pin controls the operation phase and the current consumption of ZSSC3281. Within the active phase of Sleep Mode, a subsets of serial interface commands are supported, new measurement can be started, and results can be gathered. During the power save phase no communication is possible and ZSSC3281 stays in power down phase to allow the lowest possible current consumption.

ZSSC3281 provides a fourth operation mode which is not a user accessible operation mode:

Boot/Diagnosis Mode	Boot Mode: this is immediately active after power-on or reset of ZSSC3281, while the firmware is still in boot-up phase and the Command Interpreter is not functional yet. The serial interfaces are only partly operational in Boot/Diagnosis Mode to allow an external host to read the system status for ZSSC3281. Write access and command execution is not supported.
----------------------------	-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

Diagnosis Mode: this indicates the Static Diagnostic Mode (SDM) of the firmware and it is reached if the system self-supervision detects either of the following system faults that could lead to unreliable or unpredictable behavior of the IC:

- 2 bit SRAM failures
- Internal ARM faults (bus failures, ALU failures, memory or command failures)
- CRC failures of CCP page
- First time that watchdog triggers

In the SDM mode the autonomous, cyclically repeated sensor measurements running in Cyclic Mode are stopped and the analog output is set to LDR, digital outputs (PWM, FOUT, ALARM) are set to high-Z, and CLOCK_OUT remains active.

Leaving SDM is possible via watchdog reset or power cycle.

Within SDM, the operation mode and the memory error flag inside the status flag is set supporting the detection of Boot or Diagnosis Mode.

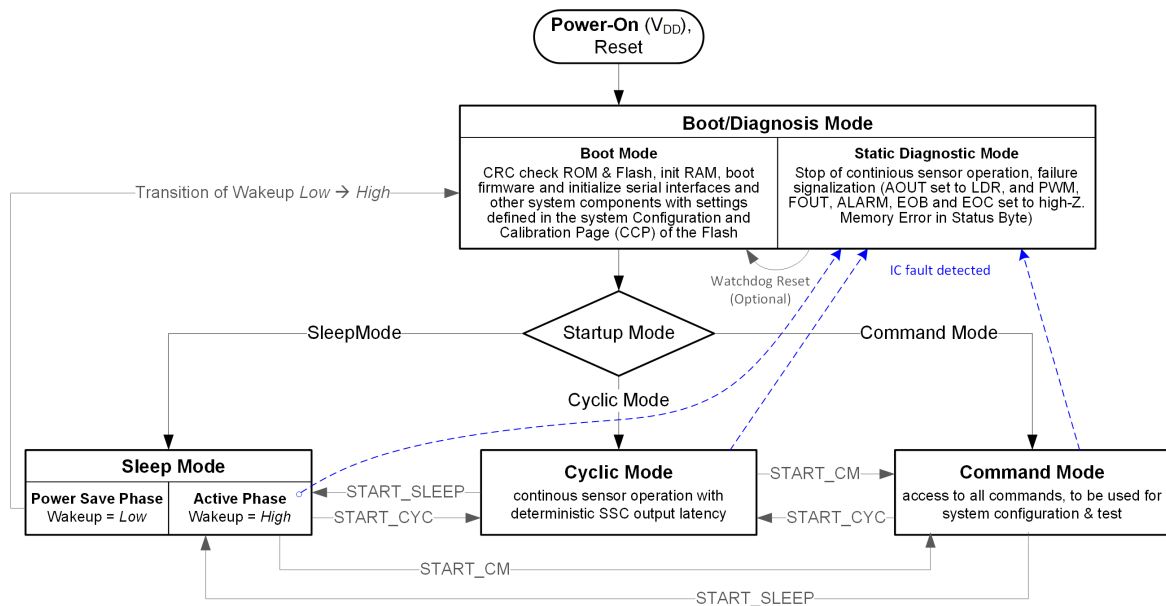


Figure 5: Main Operating Modes

After power-on (reset) the ZSSC3281 always enters the programmed System Startup Mode (GUI path: Configure\System Control\System Startup) as soon as the firmware boot process is finished.

Each of the three operating modes can be set up as the default startup mode. Changing the ZSSC3281 to another operating mode is possible via the mode change and start commands: START_CM, START_CYC and START_SLEEP (see subsection 10.5 for details).

The ZSSC3281 supports three different types of digital interfaces: I2C/I3C, SPI, and OWI. All three interface types are available in the different main operating modes if they were enabled via GUI.

3.2 System Clocks

3.2.1 Internal Oscillators and Specifications

ZSSC3281 is equipped with two internal oscillators:

- Calibrated, first order temperature compensated 16MHz system clock oscillator
- Un-calibrated, first order temperature compensated 32kHz ultra low power oscillator

3.2.2 Main System Clock

The Main System Clock, which drives the ARM MCU, the memories (ROM, Flash, SRAM), and the peripherals is derived from the internal System Clock Oscillator. By default, the oscillator frequency (16MHz) is directly applied across the entire system without further down division. Hardware and software driven clock gating are applied to maintain a low power consumption.

For applications where power consumption of ZSSC3281 is a concern, the Main System Clock can be reduced by choosing a system clock source divider other than the value of div1. The maximum divider factor can be 16 (div16), which sets the Main System Clock to 1MHz.

The system clock divider can be changed via GUI field: Configure\PowerSupply and Oscillator\System Clock Source Divider.

If the ZSSC3281 is operated in a 2-Wire Current Loop setup (and respective GUI configurations are made) a reduction of the Main System Clock to 1 MHz is mandatory to meet the maximum system current consumption specification (<4mA) over the entire temperature range. In this case the 'System Clock Source Divider' is not selectable by the user.

3.2.3 Always-On Clock

The 32kHz always-on clock is used by the System Management Unit to control the power-up-sequence of the ZSSC3281 device, as well as by the internal watchdog and the low speed timer.

3.3 System Reset

The ZSSC3281 becomes reset at following scenarios:

- Power On Reset Voltage at VDD or VDDD is below limits as specified in subsection 2.4.
- External Reset RESN Pin of ZSSC3281 is set to LOW.
- Self-Reset Self supervision via system diagnosis detected a critical system state and sets system in safe reset state.

Table 15: VDDD Power-On-Reset Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{riseVDDD}	reset release voltage	VDDD level where reset is released	1.35		1.8	V
V_{fallVDDD}	reset voltage	VDDD level where reset is generated	1.1		1.6	V
V_{hysVDDD}	reset hysteresis voltage		50		500	mV

4 Analog Front End (AFE)

The ZSSC3281 features two fully independent Analog Front Ends (AFEs), each capable of measuring both resistive and capacitive sensor elements.

4.1 AFE Signal Path

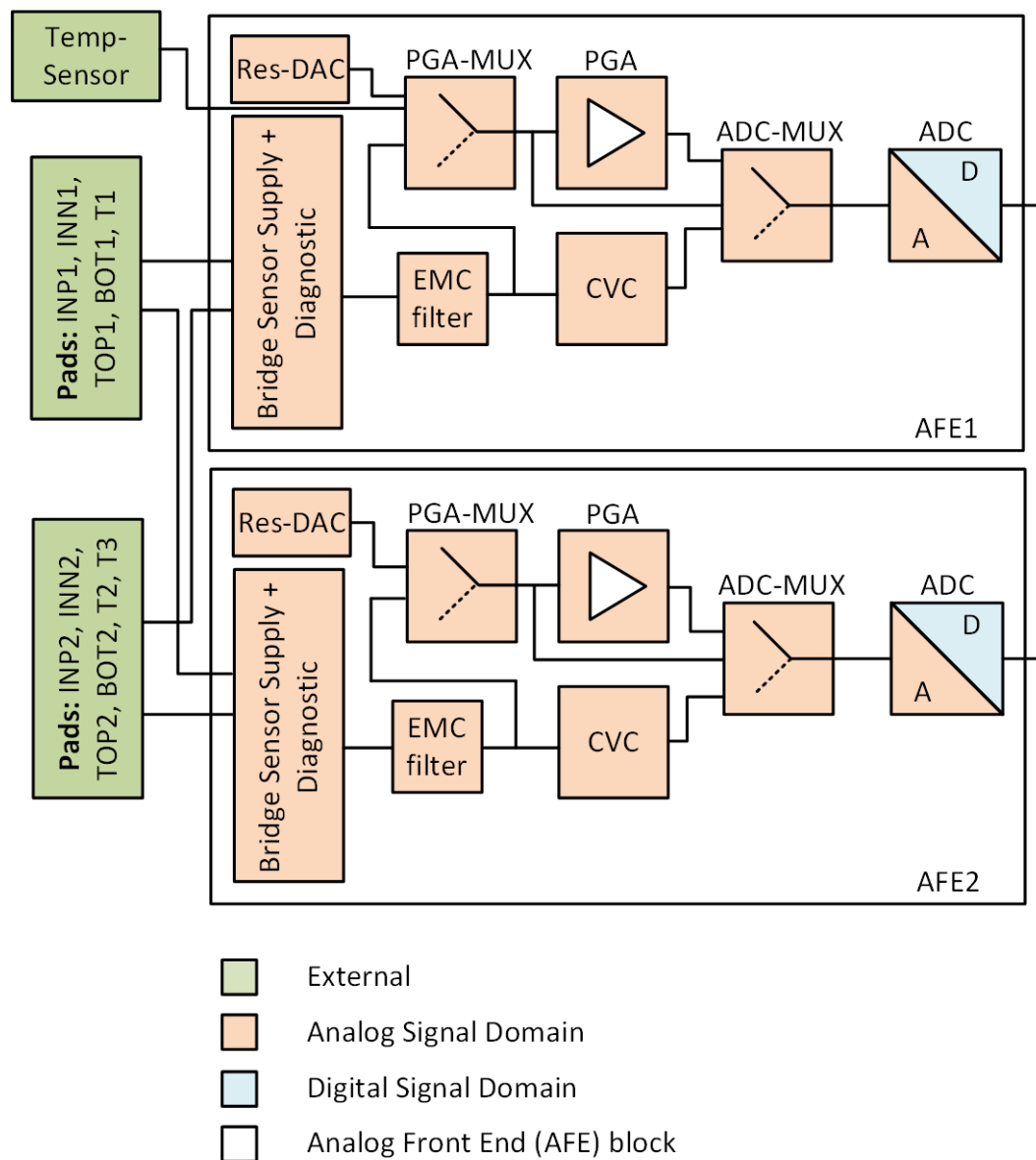


Figure 6: Block Diagram Analog Front End

4.2 Resistive Bridge Sensors

Table 16: Resistive Bridge Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_{br}	Bridge resistor	Constant Voltage Mode	0.825		60	k Ω
		Constant Current Mode	0.1			
C_{br}	Bridge capacitance, depends on the required resolution: $\tau = R_{br} \times C_{br}$ defines the settle time.	Filter capacitance C_{br} between INN x /INP x and VSS		1		nF
V_{sig}	Signal span	mV/V is related to the bridge supply			500	mV/V
V_{off}	Signal offset	For example: $V_{sig} = 1\text{mV}$ allows $V_{off} = 20\text{mV}$			2000	% off V_{sig}
					20	1/ V_{sig}

Table 17: Resistive Bridge Application Configurations

Type #	Application Case	AFE1	AFE2	Comment
1	One resistive sensor	Resistive sensor 1	-	
2	Two resistive sensors	Resistive sensor 1	Resistive sensor 2	Not available with 2-wire current loop operation
3	One resistive sensor at both inputs	Resistive sensor 1 (normal speed)	Resistive sensor 1 (low speed)	Not available with 2-wire current loop operation

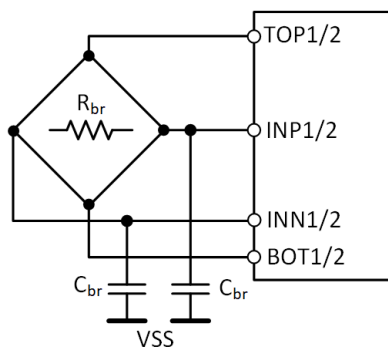


Figure 7: Bridge Sensor Type 1

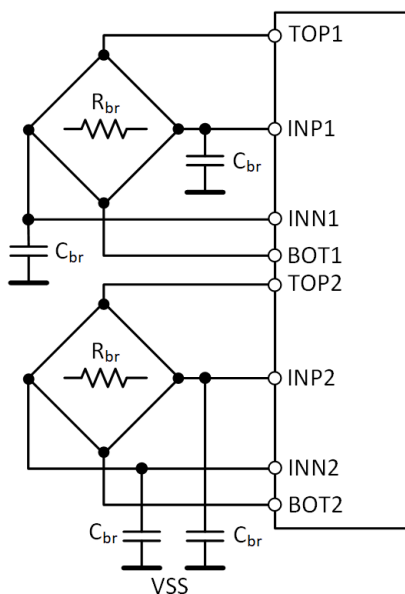


Figure 8: Bridge Sensor Type 2

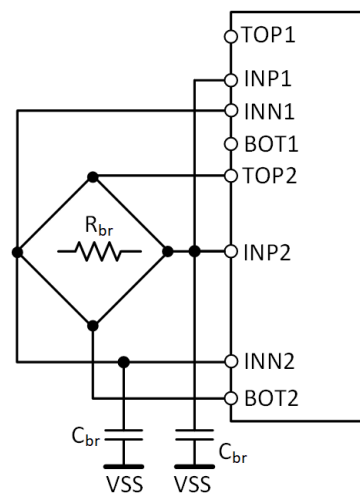
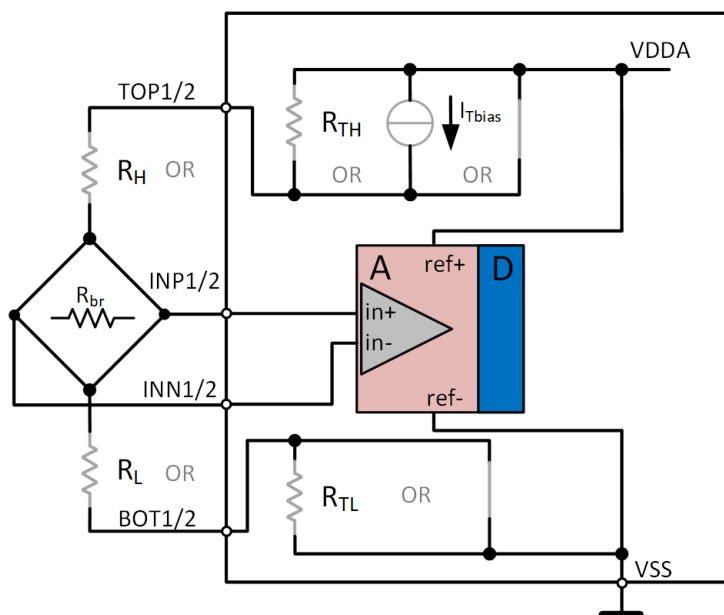


Figure 9: Bridge Sensor Type 3

In single bridge applications shown in Figure 7 the resistive bridge can be connected to either AFE1 or AFE2 depending on the PCB layout requirements.

The resistive bridge can be sourced either in Constant Voltage mode (V-source) or in Constant Current mode (I-source).

Note: Constant Current mode requires a low bridge resistance for optimal performance.



Legend:

Gray components: can be activated “either-or” via the GUI.

Figure 10: Resistive Bridge Bias Configurations

In Constant Current mode the bridge output must be set within the common input range of the PGA. This can be done with a low side external resistor R_L or with the internal resistor R_{TL} . The current that is supplied to the bridge must be adjusted to the bridge resistance. To align with the common input range of the PGA, adjust the R_L or the internal R_{TL} as needed.

In Constant Voltage mode the bridge current can be reduced by inserting the internal high and low side resistors R_{TH} , R_{TL} or by adding external resistors R_H and R_L .

Table 18: Resistive Bridge Supply Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{TOP1/2}$	Output voltage at TOP1/2			VDDA		V
I_{load}	Load current	In Constant Voltage mode defined by bridge resistance			2	mA
I_{Rbr_bias}	Current out of TOP1/2	In Constant Current mode adjustable via <i>BmBrdgIBias</i>	5		500	μ A
C_{TOP_BOT}	Load capacitance				2.2	nF
R_{TH}, R_{TL}	Bias resistor		1.3		40	k Ω

4.3 Capacitive Sensors

Note: External temperature sensor 2 is unavailable in capacitive mode, and External temperature sensor 3 is also unavailable when the shield driver for AFE2/CVC2 is enabled in specific operating modes.

Table 19: Parameter Capacitive FE

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
C _{RES}	Result resolution		10		24	bit
t _{C_AOUT SR}	Step response 2 * (AZs + SM + aux)	AFE speed, no shield driver, noise mode normal, temperature sensor ADC resolution ≤12bit capacitive sensor ADC resolution				ms
		12bit		1.04		
		14bit		1.85		
		16bit		3.48		
t _{C_CONV}	conversion time for AZS + SM + aux	normal AFE speed, no shield driver, noise mode normal, temperature sensor ADC resolution ≤12bit				ms
		12bit		0.54		
		14bit		0.94		
		16bit		1.75		
C _x , C _y , C _r	input parameter/capacitances	see CVC parameter Table 31				

Table 20: Capacitive Application Configurations

Mode	Application case	AFE1	AFE2	Comment
1	Single Ended / Fully Isolated	x		
2	Single Ended + External Reference / Fully Isolated	x		
3	Differential / Fully Isolated	x		
4	Single ended / Referred to Ground	x		
5	Single ended + External Reference / Referred to Ground	x	x	
6	Differential / Referred to Ground	x		
11	Differential (C _x -C _y)/(C _x +C _y) / Referred to Ground	x	x	

Refer to subsection 4.9 for detailed descriptions of the different application modes.

To optimize measurement performance, the following configuration options are available:

- AFE Speed Reduction: Recommended for certain application modes to ensure measurement accuracy (see Table 22 and Table 23).
- Shield Driver: In ground-referenced systems, enabling the shield driver reduces stray capacitance and improves signal integrity (see Table 21).
- Noise Modes: Two selectable modes that influence sample rate, conversion time, and step response (see Table 24 to Table 30).

Note: These settings directly impact measurement accuracy and timing.

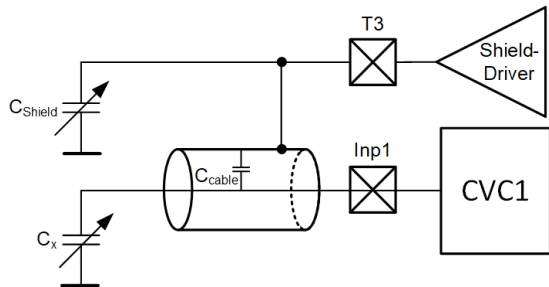


Figure 11: CVC Shield Driver Mode

Table 21: CVC Shield Mode

Mode	CmXEnShieldDrv	CmShieldDriver10nF
no shield driver	0	0
1nF driver mode	1	0
10nF driver mode	1	1

Table 22: Application Modes 1 to 3 AFE Speed Reduction

	Required AFE Speed Reduction	
	C_x and C_y	Application Mode 1-3
	<40 pF	2x
	<80 pF	4x

Table 23: Application Modes 4 to 11 AFE Speed Reduction

	Required AFE Speed Reduction	
	C_x and C_y	Application Mode 4-11
	<50 pF	<100 pF
Application Mode 4-11, no shield driver	1x	2x
Application Mode 4-11, 1nF shield driver	4x	4x
Application Mode 4-11, 10nF shield driver	2x	4x

Table 24: Noise Mode

CmNoiseMode
Normal
Low Noise

Table 25: Performance Capacitive Front End, AFE Speed Reduction Factor = 1, Cm10nFShieldEn = 0

ADC res/bit	ADC clks	Normal	Low Noise	Normal	Low Noise	Normal	Low Noise	If C _{int} =20pF and 2x ADC Gain enabled
		Conversion Time/ μ s		Sample Rate/Hz		Step Response Time/ms		Resolution fF/LSB
10	64	301	1016	3322	984	0.60	2.03	19.53
11	91	404	1405	2475	712	0.80	2.80	9.77
12	128	535	1939	1869	516	1.04	3.85	4.88
13	182	706	2695	1416	371	1.39	5.36	2.44
14	256	936	3731	1068	268	1.85	7.44	1.22
15	364	1278	5243	782	191	2.53	10.46	0.61
16	512	1751	7315	571	137	3.48	14.60	0.31
17	728	2435	10339	411	97	4.84	20.65	0.15
18	1024	3368	14483	297	69	6.71	28.94	0.0763
19	1456	4736	20531	211	49	9.45	41.04	0.0381
20	2048	6615	28819	151	35	13.20	57.61	0.0191
21	2912	9351	40915	107	24	18.68	81.80	0.0095
22	4096	13096	57491	76	17	26.17	114.96	0.0048
23	5824	18568	81683	54	12	37.11	163.34	0.0024
24	8192	26071	114835	38	9	52.12	229.64	0.0012

Table 26: Performance Capacitive Front End, AFE Speed Reduction Factor = 1, Cm10nFShieldEn = 1

ADC res/bit	ADC clks	Normal	Low Noise	Normal	Low Noise	Normal	Low Noise	If C _{int} =20pF and 2x ADC Gain enabled
		Conversion Time/ μ s		Sample Rate/Hz		Step Response Time/ms		Resolution fF/LSB
10	64	521	2336	1919	428	1.04	4.67	19.53
11	91	724	3265	1381	306	1.44	6.52	9.77
12	128	975	4539	1026	220	1.92	9.05	4.88
13	182	1326	6375	754	157	2.63	12.72	2.44
14	256	1796	8891	557	112	3.57	17.76	1.22
15	364	2498	12563	400	80	4.97	25.10	0.61
16	512	3471	17595	288	57	6.92	35.16	0.31
17	728	4875	24939	205	40	9.72	49.85	0.15
18	1024	6788	35003	147	29	13.55	69.98	0.0763
19	1456	9596	49691	104	20	19.17	99.36	0.0381
20	2048	13455	69819	74	14	26.88	139.61	0.0191
21	2912	19071	99195	52	10	38.12	198.36	0.0095
22	4096	26756	139451	37	7	53.49	278.88	0.0048
23	5824	37988	198203	26	5	75.95	396.38	0.0024
24	8192	53391	278715	19	4	106.76	557.40	0.0012

Table 27: Performance Capacitive Front End, AFE Speed Reduction Factor = 2, Cm10nFShieldEn = 0

ADC res/bit	ADC clks	Normal	Low Noise	Normal	Low Noise	Normal	Low Noise	If C _{int} =20pF and 2x ADC Gain enabled
		Conversion Time/μs		Sample Rate/Hz		Step Response Time/ms		Resolution fF/LSB
10	64	602	2032	1661	492	1.14	4.00	19.53
11	91	808	2810	1238	356	1.53	5.53	9.77
12	128	1070	3878	935	258	2.02	7.63	4.88
13	182	1412	5390	708	186	2.70	10.66	2.44
14	256	1872	7462	534	134	3.62	14.80	1.22
15	364	2556	10486	391	95	4.99	20.85	0.61
16	512	3502	14630	286	68	6.88	29.14	0.31
17	728	4870	20678	205	48	9.62	41.23	0.15
18	1024	6736	28966	148	35	13.35	57.81	0.0763
19	1456	9472	41062	106	24	18.82	82.00	0.0381
20	2048	13230	57638	76	17	26.34	115.15	0.0191
21	2912	18702	81830	53	12	37.28	163.54	0.0095
22	4096	26192	114982	38	9	52.26	229.84	0.0048
23	5824	37136	163366	27	6	74.15	326.61	0.0024
24	8192	52142	229670	19	4	104.16	459.22	0.0012

Table 28: Performance Capacitive Front End, AFE Speed Reduction Factor = 1, Cm10nFShieldEn = 1

ADC res/bit	ADC clks	Normal	Low Noise	Normal	Low Noise	Normal	Low Noise	If C _{int} =20pF and 2x ADC Gain enabled
		Conversion Time/μs		Sample Rate/Hz		Step Response Time/ms		Resolution fF/LSB
10	64	1042	4672	960	214	2.02	9.28	19.53
11	91	1448	6530	691	153	2.81	12.97	9.77
12	128	1950	9078	513	110	3.78	18.03	4.88
13	182	2652	12750	377	78	5.18	25.38	2.44
14	256	3592	17782	278	56	7.06	35.44	1.22
15	364	4996	25126	200	40	9.87	50.13	0.61
16	512	6942	35190	144	28	13.76	70.26	0.31
17	728	9750	49878	103	20	19.38	99.63	0.15
18	1024	13576	70006	74	14	27.03	139.89	0.0763
19	1456	19192	99382	52	10	38.26	198.64	0.0381
20	2048	26910	139638	37	7	53.70	279.15	0.0191
21	2912	38142	198390	26	5	76.16	396.66	0.0095
22	4096	53512	278902	19	4	106.90	557.68	0.0048
23	5824	75976	396406	13	3	151.83	792.69	0.0024
24	8192	106782	557430	9	2	213.44	1114.74	0.0012

Table 29: Performance Capacitive Front End, AFE Speed Reduction Factor = 4, Cm10nFShieldEn = 0

ADC res/bit	ADC clks	Normal	Low Noise	Normal	Low Noise	Normal	Low Noise	If C _{int} =20pF and 2x ADC Gain enabled
		Conversion Time/ μ s		Sample Rate/Hz		Step Response Time/ms		Resolution fF/LSB
10	64	1204	4064	831	246	2.20	7.92	19.53
11	91	1616	5620	619	178	2.98	10.99	9.77
12	128	2140	7756	467	129	3.96	15.20	4.88
13	182	2824	10780	354	93	5.33	21.24	2.44
14	256	3744	14924	267	67	7.17	29.53	1.22
15	364	5112	20972	196	48	9.91	41.63	0.61
16	512	7004	29260	143	34	13.69	58.20	0.31
17	728	9740	41356	103	24	19.16	82.40	0.15
18	1024	13472	57932	74	17	26.63	115.55	0.0763
19	1456	18944	82124	53	12	37.57	163.93	0.0381
20	2048	26460	115276	38	9	52.60	230.24	0.0191
21	2912	37404	163660	27	6	74.49	327.00	0.0095
22	4096	52384	229964	19	4	104.45	459.61	0.0048
23	5824	74272	326732	13	3	148.23	653.15	0.0024
24	8192	104284	459340	10	2	208.25	918.36	0.0012

Table 30: Performance Capacitive Front End, AFE Speed Reduction Factor = 1, Cm10nFShieldEn = 1

ADC res/bit	ADC clks	Normal	Low Noise	Normal	Low Noise	Normal	Low Noise	If C _{int} =20pF and 2x ADC Gain enabled
		Conversion Time/ μ s		Sample Rate/Hz		Step Response Time/ms		Resolution fF/LSB
10	64	2084	9344	480	107	3.96	18.48	19.53
11	91	2896	13060	345	77	5.54	25.87	9.77
12	128	3900	18156	256	55	7.48	36.00	4.88
13	182	5304	25500	189	39	10.29	50.68	2.44
14	256	7184	35564	139	28	14.05	70.81	1.22
15	364	9992	50252	100	20	19.67	100.19	0.61
16	512	13884	70380	72	14	27.45	140.44	0.31
17	728	19500	99756	51	10	38.68	199.20	0.15
18	1024	27152	140012	37	7	53.99	279.71	0.0763
19	1456	38384	198764	26	5	76.45	397.21	0.0381
20	2048	53820	279276	19	4	107.32	558.24	0.0191
21	2912	76284	396780	13	3	152.25	793.24	0.0095
22	4096	107024	557804	9	2	213.73	1115.29	0.0048
23	5824	151952	792812	7	1	303.59	1585.31	0.0024
24	8192	213564	1114860	5	1	426.81	2229.40	0.0012

Table 31: Parameter CVC

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
C_{shift}	Internal shift capacitance	Programmable in 31 steps, step size 2pF	0		62	pF
C_{int}	Internal reference capacitance	Programmable in 31 steps, step size 2pF	20		82	pF
C_{offset}	Compensate-able absolute sensor offset	For single ended input, single cap. C_x		C_{shift}		
$\text{ERR}_{\text{rel } C_{\text{int}}}$	Measurement error C_{int}	Application Mode 1, 2, 3, 4, 5, 6 and 11	-1		1	%
$\text{ERR}_{\text{rel } C_{\text{shift}}}$	Measurement error C_{shift}	Application Mode 1, 2, 4, 5 and 11	-1		1	%
		Application Mode 3 and 6 C_{shift} is effectively not trimmed	-15		15	
C_{shield}	Capacitive load at shield driver to GND	Driver mode 1nF	0.05		1	nF
		Driver mode 10nF	1		10	
C_{cable}	Capacitance between shield and C_x , C_r (cable capacitance) see also Table 21				500	pF

4.4 Auxiliary Temperature Sensor Inputs

4.4.1 Internal PTAT Temperature Sensor

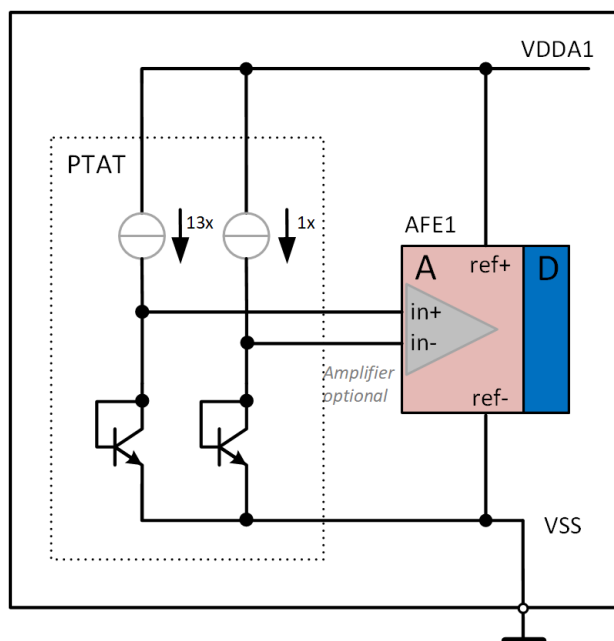


Figure 12: PTAT Sensor Configuration

Table 32: Internal PTAT Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
T_{meas}	Measurement range		-55		125	°C
E_T	Measurement error	Calibrated	-5		5	K
ADC_{res}	Resolution	Programmable ADC resolution	10		15	bit
T_{res}	Effective resolution	$\pm 1.5\sigma$	2			LSB/°C
S	Sensitivity	Differential output voltage	218		230	$\mu\text{V/K}$

4.4.2 External Temperature Sensors

Three different external sensor types can be used to measure the temperature of the main sensor or a media temperature in the auxiliary signal path of the AFEs:

- PTC
- Diode
- TC Bridge Sensor

The PTC and Diode Sensors can be supplied either in Sink Mode or in Source Mode as shown in Figure 13. The gray marked components can be activated “either-or” via the GUI. The AGND potential is at $VDDA/2$.

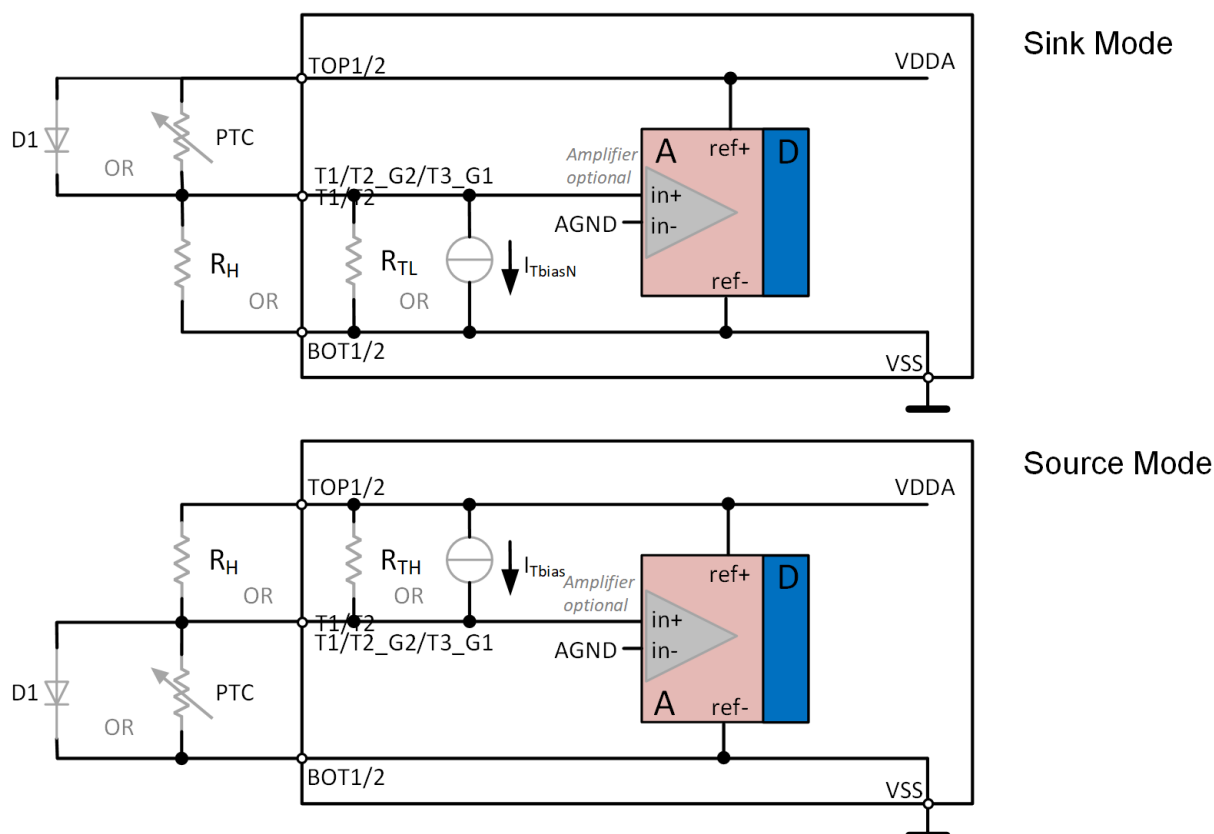
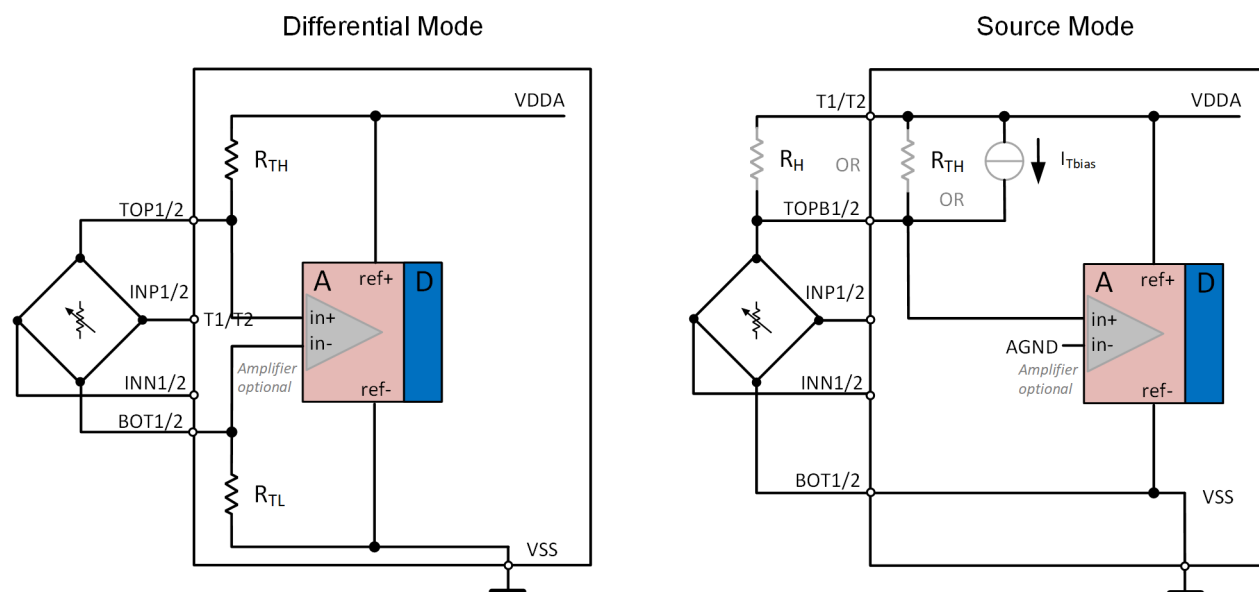


Figure 13: PTC, Diode Sensor Bias Configurations

TC Bridge Sensor configurations can be supplied in Differential Mode or Source Mode as shown in Figure 14.



Legend:

Gray components: can be activated "either-or" via the GUI. The AGND potential is at $VDDA/2$.

Figure 14: TC Bridge Sensor Bias Configurations

Table 33: External Temperature Sensor Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_{sensor}	Sensor resistance (PTC/TC Bridge Sensor)		50		1M	Ω
ADC_{res}	ADC resolution	Programmable ADC resolution	10		15	bit
ENOB	Effective resolution	$\pm 1.5\sigma$	14			bit

4.5 Programmable Gain Amplifier (PGA)

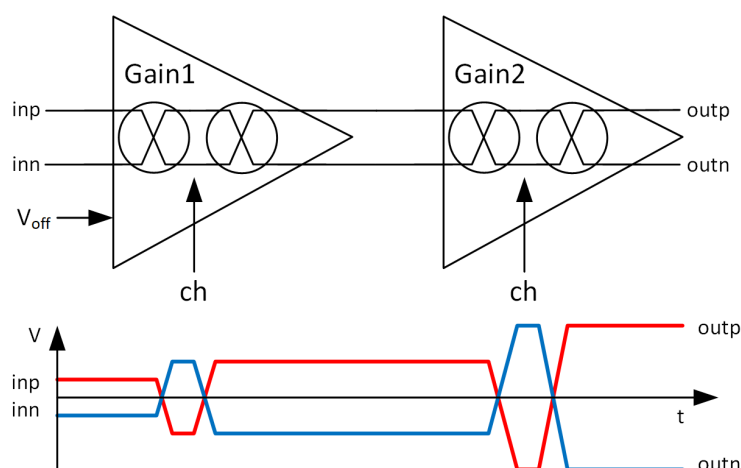


Figure 15: PGA Architecture

The first amplifier (Gain1) has a built in PGA offset compensation (auto-zero) that is refreshed at the beginning of every measurement. The second stage has no offset compensation. The second stage amplifier offset is present at the PGA output with offset \times Gain2. Both PGA amplifier stages have built-in chopper functionality to suppress $1/f$ noise.

The gain settings that can be selectively programmed for both PGA stages are listed in Table 34.

Table 34: PGA Gain Steps

Gain1	Gain2
1.2	1.1
2	1.2
4	1.3
5.97	1.4
11.9	1.5
19.8	1.6
29.6	1.7
39.2	1.8
58.1	
76.6	
112	
143	
187	
223	
275	

If bridge sensors show noticeable DC offsets (that is offset from 0) in their differential output voltage, it restricts the maximum PGA gain that can be applied without causing saturation. To compensate this, the PGA can be programmed to shift the input signal by an offset voltage, as shown in the Figure 16. The default shift is 0mV, and the offset can be adjusted in 15 steps in both positive and negative directions, see Table 34 and Table 35. This PGA offset shift function is available only for PGA Gain values of 11.9 or higher.

Table 35: PGA Input Offset Compensation Steps

$11.9 \leq \text{Gain1} \leq 223$ [mV]	Gain1 = 275 [mV]
0	0
±1.9	±1.5
±3.8	±3
±5.6	±4.5
±7.5	±6
±9.4	±7.5
±11.3	±9
±13.1	±10.5
±15	±12
±16.9	±13.5
±18.8	±15
±20.6	±16.5
±22.5	±18
±24.4	±19.5
±26.3	±21
±28.1	±22.5

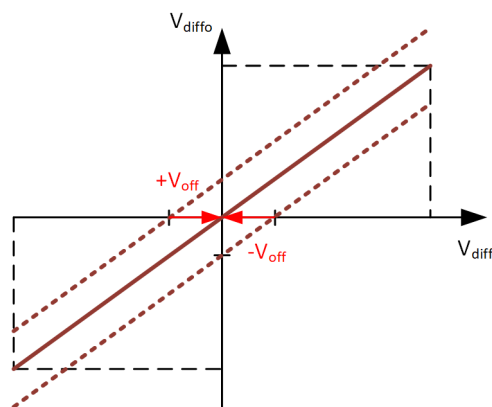


Figure 16: PGA Input Offset Compensation

PGA gain and the Input Offset Compensation value can be programmed separately for the two main bridge sensors and for the three external auxiliary temperature sensors that can be connected to the ZSSC3281. The PGA Input Offset Compensation feature is limited to SM+/SM- and SM+ sequencer configurations which are described in subsection 4.7.

Table 36: PGA Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
Gain	Total PGA gain	Programmable in 15/8 steps: • stage1: 15 steps, 1.2 to 275 • stage2: 8 steps, 1.1 to 1.8	1.32		495	V/V
V _{cmi}	Input Common Mode voltage			VDDA/2		V
BW _{PGA}	Bandwidth			5		kHz
t _{az_PGA}	Auto-zero time		10			μs
f _{ch_PGA}	Chopper frequency			100		kHz

4.6 Analog-to-Digital Converter (ADC)

An incremental delta-sigma analog-to-digital converter (ADC) is used to digitize the PGA signal. To allow optimizing the trade-off between conversion time and resolution, the resolution can be programmed from 10-bit to 24-bit. The ADC processes differential input signals around its input Common Mode level VDDA/2. Table 37 lists the ADC resolution, signal ranges, conversion times for a single analog-to-digital conversion and VDDA = 1.65V.

Table 37: ADC Configuration Parameters

ADC Resolution [Bits]	Full Scale Input Voltage V _{fs} [V]	LSB Size V _{LSB} [μV]	Conversion Time, Typical, T _{Conv} [μs]	Conversion Rate, Typical, F _{Conv} [kHz]
10	±1.418	2768.638	32.54	30.73
11	±1.425	1391.718	43.75	22.86
12	±1.431	698.499	59.59	16.78
13	±1.434	350.189	81.99	12.20
14	±1.437	175.428	113.68	8.80
15	±1.439	87.832	158.49	6.31
16	±1.440	43.958	221.86	4.51
17	±1.441	21.994	311.48	3.21
18	±1.442	11.002	438.22	2.28
19	±1.443	5.503	617.46	1.62
20	±1.443	2.752	870.94	1.15
21	±1.443	1.376	1229.41	0.81
22	±1.443	0.688	1736.38	0.58
23	±1.443	0.344	2453.33	0.41
24	±1.444	0.172	3467.25	0.29

The ADC can perform an additional offset shift (independent of the PGA shifting) to adapt input signals with offsets to the ADC input range. Enabling the offset shift causes the ADC to perform an additional amplification of the ADC's input signal by factor ×2. This must be considered for a correct PGA configuration setup.

The ADC offset shift feature is limited to SM+/SM- and SM+ sequencer configurations which are described in subsection 4.7.

The shift values in Table 38 are related to the input voltages at INP, INN:

- Full scale differential input voltage: $V_{INdiff_fs} = \frac{V_{fs}}{Gain}$
- Differential input shift voltage: V_{INdiff_shift}
- Maximum, minimum differential input voltage: V_{INdiff_max} , V_{INdiff_min}

Table 38: ADC Input Offset Shift Steps

PGA Polarity	ADC Shift Enable	ADC Gain	ADC Shift	$V_{INDIFF_shift}/V_{INDIFF_fs}$	$V_{INDIFF_min}/V_{INDIFF_fs}$	$V_{INDIFF_max}/V_{INDIFF_fs}$
Positive	0	x1	0	No shift	-1	+1
Negative			0	No shift	+1	-1
Positive	1	×2	1	7/8	-1/16	+15/16
			2	6/8	-2/16	+14/16
			3	5/8	-3/16	+13/16
			4	4/8	-4/16	+12/16
			5	3/8	-5/16	+11/16
			6	2/8	-6/16	+10/16
			7	1/8	-7/16	+9/16
			0	No shift	-1/2	+1/2
Negative			0	No shift	+1/2	-1/2
			1	1/8	-9/16	+7/16
			2	2/8	-10/16	+6/16
			3	3/8	-11/16	+5/16
			4	4/8	-12/16	+4/16
			5	5/8	-13/16	+3/16
			6	6/8	-14/16	+2/16
			7	7/8	-15/16	+1/16

4.7 AFE Sequencer

The measurement flow, especially the frequency of main bridge measurements vs. auxiliary measurements can be configured by the user. Once started by the ARM MCU, the measurement flow runs autonomously controlled by the AFE. The AFE Sequencer state machine ensures predictable measurement timing in the continuous cyclic operation of ZSSC3281.

The AFE sequencer carries out AFE measurements based on a measurement slot mechanism. There can be up to eight measurement slots assigned per AFE, which form a single measurement cycle. A measurement cycle can be executed only once (for example, initiated by a dedicated command request) or continuously cycled in Cyclic Mode operation of ZSSC3281.

Each of the measurement slots inside AFE1 or AFE2 can be individually configured for the following measurement types:

- Sensor Measurement (SM+): bridge inputs INP/INN directly converted (non-inverted)
- Sensor Measurement (SM-): bridge inputs INP/INN flipped (inverted)
- Auxiliary Measurement (aux_i): cycles through the auxiliary measurement vector

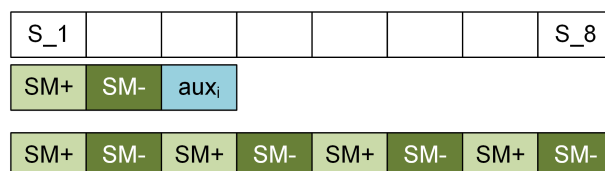


Figure 17: Measurement Slot Configuration with Two Example Configurations

The actual number of measurement slots per measurement cycle can be defined by the user between 1 and 8. The hardware allows to configure any combination, but not all combinations lead to reasonable measurement schemes. The GUI supports the user in selecting proper measurement schemes. Figure 17 shows two example configurations. The measurement schemes are explained in further detail in subsubsection 4.7.3, 4.7.4, and 4.7.5.

Auxiliary measurements usually have lower response time requirements than measurements on the main sensor bridge. The auxiliary measurements are therefore cycled orthogonal to the main loop of the sequencer. Activated

auxiliary measurements become listed in the so called auxiliary measurement vector. The vector index 'i' gets increased after each executed aux_i slot and starts over after the entire set of active measurements was completed. The configuration options of auxiliary measurements are further detailed in subsubsection 4.7.2.

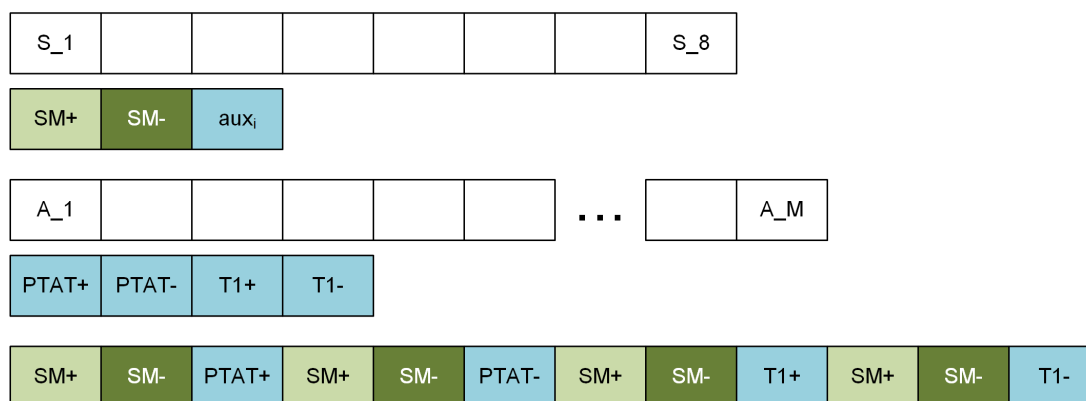


Figure 18: Auxiliary Measurement Configuration, and Corresponding Measurement Flow

Figure 18 illustrates the sequencer operation with an example configuration using 4 auxiliary measurements. During the 3rd measurement (configured as aux_i), the first enabled auxiliary measurement is executed ("PTAT", internal temperature sensor). After the measurement sequence (SM+/SM-/ aux_i) is executed again in the next measurement slot, the next enabled auxiliary measurement is executed ("T1", external temperature sensor). Similarly, "Bridge1 open" and "Bridge1 short" diagnostics measurements are carried out in following measurement slots. During the 5th execution of the measurement sequence, the PTAT auxiliary measurement is carried out again.

4.7.1 Bridge Sensor Measurement Configuration

The main bridge sensor signals can be measured in three ways:

- SM+/SM- (or SM-/SM+) measurement
- SM+/AZ measurement (SM+ and auto-zero measurement)
- SM+ without AUX_AZ measurement

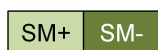


Figure 19: SM+/SM- (or SM-/SM+) Measurement



Figure 20: SM+/AZ Measurement

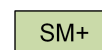


Figure 21: SM+ without AZ Measurement

Configurations in Figure 19 and Figure 20 provide digital offset compensation of the entire signal path in the analog front end. The configuration in Figure 21 only provides analog offset compensation in the first stage of the PGA. The offsets of the second PGA stage and the ADC offset are not compensated.

In the SM+/SM- configuration, the bridge inputs INP/INN are first converted straight forward in the SM+ measurement slot and second with an internally flipped INP/INN input signal in SM- slot. For the SM+/AZ configuration, the second measurement (AZ) is performed without applied input signal. INP/INN become disconnected from the sensor and internally shorted for AZ measurements.

Since signal integration time in SM+/SM- configuration is twice as long as in in the SM+/AZ configuration (same ADC resolution settings assumed), the SM+/SM- configuration achieves approx. 0.5 bit better noise performance than the SM+/AZ configuration. The longer input signal integration time of the SM+/SM- configuration leads to an increased output update rate and step response as described in subsubsection 4.7.3 and subsubsection 4.7.4.

The auto-zero measurement (AZ) belongs to the group of auxiliary measurements and is cycled less often if either of the following options appears:

- further auxiliary measurements are enabled in the auxiliary measurement vector described in subsubsection 4.7.2
- accelerated bridge measurements are enabled as described in subsubsection 4.7.5

Since the offset in the internal signal path varies rather slowly, the auto-zero compensation remains very accurate even for a long auxiliary measurement vector.

Because SM- needs to be configured and most sensor applications also require other auxiliary measurements, the assignment of the AZ measurement to the group of auxiliary measurements helps to reduce the worst case step response on the main bridge sensor.

The lowest step response is achieved with the “SM+ only” configuration shown in Figure 21 if no other auxiliary measurements are needed for the desired sensor application.

The input settling time of each measurement task also affects the overall measurement time, including the output update rate and worst-case response. This settling is required depending on the output resistance of the external sensors, respective capacitive loads on the signal lines and the ADC resolution selected by the user. The input settling time is always inserted before an ADC conversion starts and can be configured in the GUI for main bridge measurements via `Configure\AFE\Bridge\SetTime [μs]` and for auxiliary temperature measurements via `Configure\AFE\Temperature\SetTime [μs]`.

Considering achievable measurement latencies and noise performance, configuration shown in Figure 19 is better when higher ADC resolutions are required or for sensor configurations with fast input settling, while configuration shown in Figure 20 and Figure 21 are preferable when lower ADC resolutions become selected or for sensor configurations requiring long input settling times (bridge settling time has a considerable impact on the timing budget).

4.7.2 Auxiliary Measurement Configuration

The supported auxiliary measurements are:

- Auto-zero for internal signal path
- Temperature on sensor input T1
- Temperature on sensor input T2
- Temperature on sensor input T3
- Internal PTAT
- AFE diagnostic checks
 - Sensor connection checks for all external sensors (Short to TOPx pin or BOTx pin and Open)
 - Bridge signal range check
 - AFE gain and offset drift supervision via internal reference DAC

They can be activated in the GUI via tabs `Configure\AFE\Sequencer`, `Configure\AFE\Temperature Selection` and `Diagnostic\Sensor\AFE`.

4.7.3 Timings with SM+/SM- Configuration

As described in subsubsection 4.7.1, sensor configurations with fast input settling or applications requiring higher ADC resolutions are better served with the SM+/SM- scheme for the main bridge measurement. For the step response consideration the following application example is used:

- Sensor Measurement (non-inverted)
- Sensor Measurement (inverted)
- Auxiliary Measurement (for example, for sensor temperature)

Note: SM+ and SM- can be exchanged yielding to the same result.



Figure 22: SM+/SM- Configuration

For SM+/SM- configuration, the measurement cycle and output update rate is shown in Figure 23 for an example involving three enabled auxiliary measurement tasks. After the final main measurement task is completed, the firmware

starts data processing as detailed in section 5 and section 6. The conditioned output signal is then recorded into the output registers.

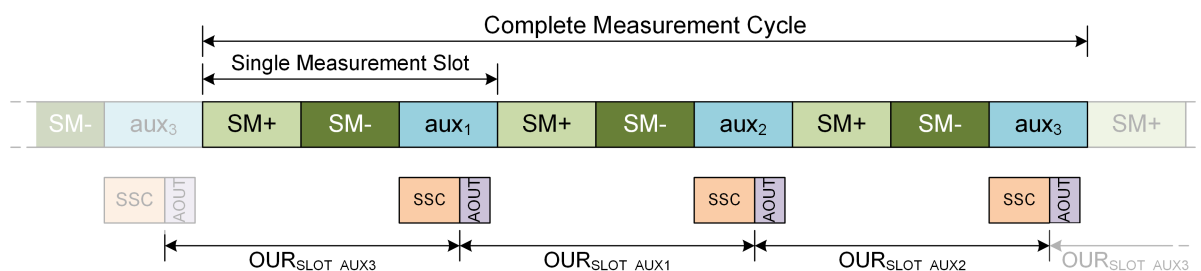


Figure 23: SM+/SM- Measurement Cycle and Output Update Rate

For SM+/SM- configuration the worst-case step response is shown in Figure 24 and consists of:

- 4 sensor ADC-conversion times (duration depending on selected ADC resolution)
- 1 auxiliary conversion time (fixed duration, based on longest auxiliary conversion timing)
- 1 SSC calculation

Additionally, there is a delay depending on the selected interface, such as the settling time at AOUT for all analog output options. In a worst-case scenario, be aware that intermediate results can occur because input changes and data readout are asynchronous to the ongoing internal measurement cycle.

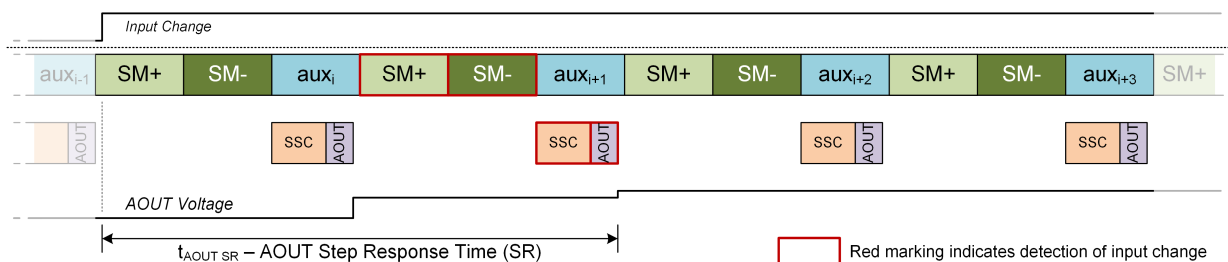


Figure 24: SM+/SM- Step Response

4.7.4 Deterministic Input Step Response with SM+/AZ Configuration

Since the SM+/SM- configuration samples the input signal twice as long as the SM+/AZ configuration and it suffers a noticeable timing overhead for sensor configurations with slow sensor input signal settling, a second SM+/AZ measurement scheme with deterministic step response times is available. For the step response consideration, the following application example is used:

- Sensor measurement (non-inverted)
- Auxiliary measurement (for example, for sensor path auto-zero and/or sensor temperature) within the auxiliary measurement vector



Figure 25: SM+/AZ Configuration

For SM+/SM- configuration, the measurement cycle and output update rate is shown in Figure 23 for an example involving three enabled auxiliary measurement tasks. After the final main measurement task is completed, the firmware starts data processing as detailed in section 5 and section 6. The conditioned output signal is then recorded into the output registers.

Assuming equal ADC resolution settings for the SM+/SM- configuration as described in subsubsection 4.7.3 and the SM+/AZ configuration described in this section, the worst case step response is shorter by two sensor AD-conversion times in case of the SM+/AZ setup. The auxiliary measurement duration in the SM+/AZ setup may become slightly longer than for the SM+/SM- configuration, since it is determined by the AZ measurement time if the selected resolution of the main bridge is larger than the resolutions of all other active auxiliary measurements. This is because the resolution of the AZ measurement is set by the resolution of the SM+ measurement and the longest measurement of the auxiliary measurement vector determines the duration of the aux_i slot(s)

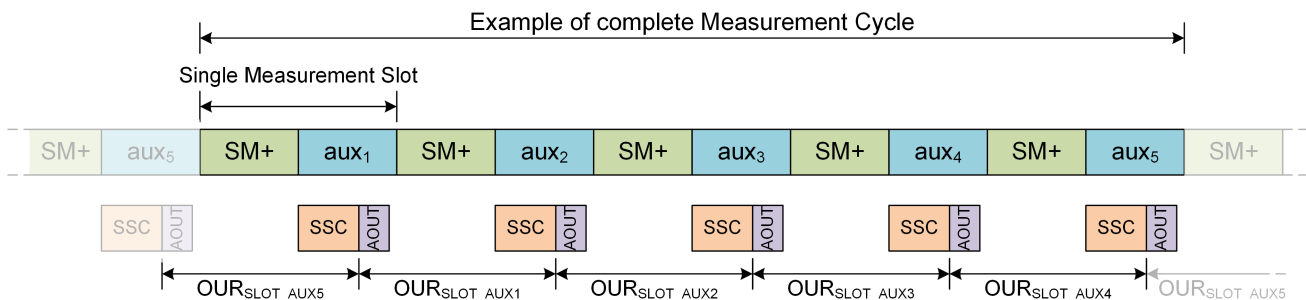


Figure 26: SM+/AZ Measurement Cycle and Output Update Rate

As shown in Figure 27, the worst-case latency consists of:

- 2 sensor AD-conversion times (duration depending on selected ADC resolution)
- 1 auxiliary conversion time (fixed duration, based on longest auxiliary conversion timing)
- 1 SSC calculation

Additionally, there is a delay depending on the selected interface, such as the settling time at AOUT for all analog output options. In a worst-case scenario, be aware that intermediate results can occur because input changes and data readout are asynchronous to the ongoing internal measurement cycle.

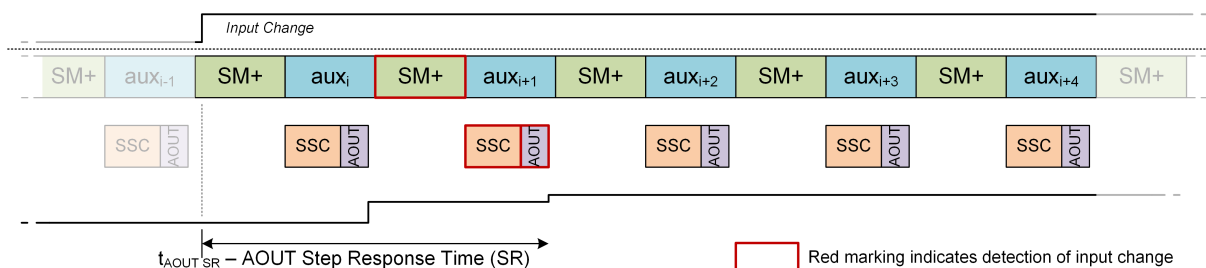


Figure 27: Measurement Flow and Latency for SM+/AZ Configuration

4.7.5 Accelerated Bridge Measurements with Sparsely Inserted Auxiliary Measurements

For applications which focus on highest conversion rates at the bridge sensor input but do not require a deterministic maximum input to output latency of the corrected sensor signal, auxiliary measurements can be sparsely inserted to occur only after a certain number of measurement sequences were executed by the AFE sequencer. This way, auxiliary measurements become executed even more seldom, giving the main sensor bridge measurements priority.

The AFE sequencer can be configured such that an aux_i measurement is only executed (inserted) after every P_x measurement sequence. P can be selected as 2, 4, or 8. Figure 28 shows an example of a measurement flow with $P = 2$ while Figure 29 uses $P = 8$ where aux_i measurements are executed after eighth measurement sequences.

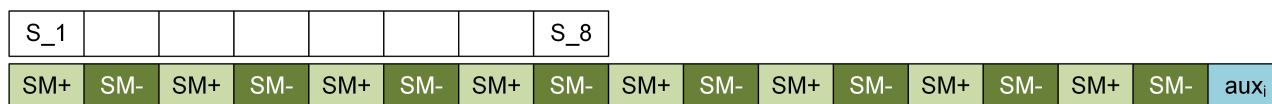


Figure 28: Auxiliary Measurement Executed after Every Second Measurement Cycle

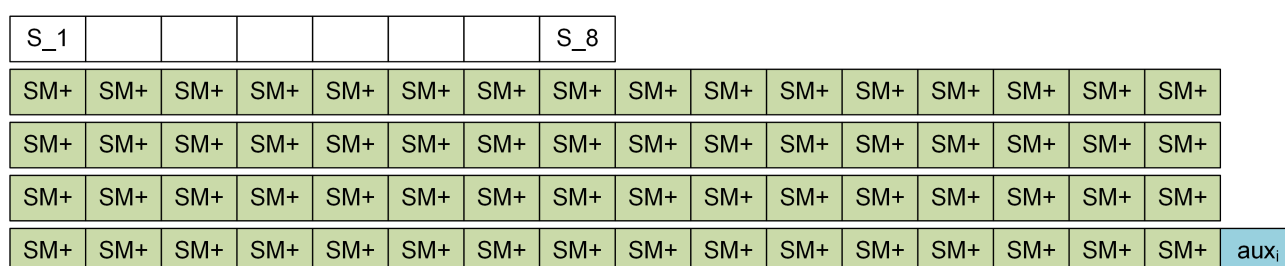


Figure 29: Sequencer Setup for Highest Update Rate on Bridge Sensor

For the SM+/SM- measurement sequencer use case, the output update rate is shown in Figure 30. The complete measurement cycle concludes after the final auxiliary measurement task is completed. Once the SM+ main measurement task is finished, the firmware starts data processing as detailed in section 5 and section 6. Since auxiliary measurement tasks are only inserted after every 2nd, 4th, or 8th measurement sequence, the output update rate varies accordingly. This explanation also applies when using only the SM+/AZ measurement sequencer.

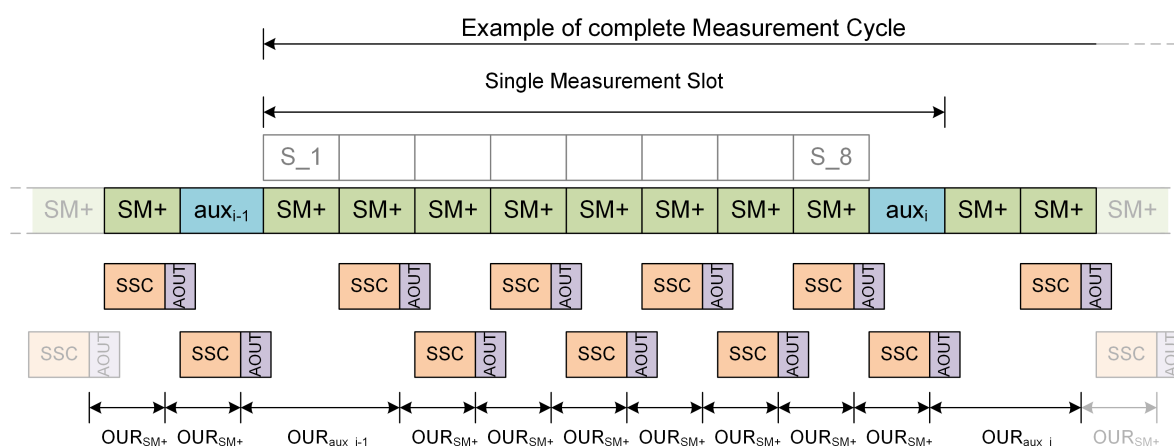


Figure 30: SM+ Accelerated Measurement Cycle and Output Update Rate

The worst-case step response primarily depends on the selected AFE sequencer mode as the following:

- SM+/SM- configuration: refer to Figure 24 and description for step response in subsection 4.7.3
- SM+/AZ configuration: refer to Figure 27 and description for step response in subsection 4.7.4

4.8 AFE Dual Speed Mode

The AFE Dual Speed Mode operation is intended for single bridge sensor applications that require a fast transient step response combined with a high resolution steady state signal at analog and serial interface outputs. It can be activated in the GUI via Configure\AFE\Sequencer\AFE Selection and Configurability\Dual speed AFE with AOUT.

In AFE Dual Speed Mode the sensor bridge is measured by both frontends (AFE1 and AFE2) in parallel, see Figure 31 for the required schematic. AFE Dual Speed Mode allows the operation of one external temperature sensor (T1) or the internal temperature sensor (PTAT).

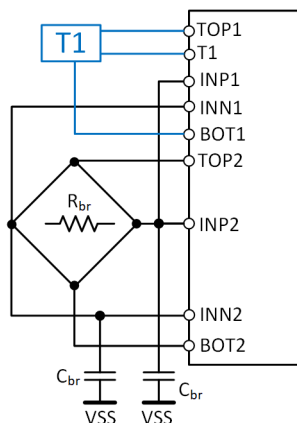


Figure 31: Schematic in AFE Dual Speed Mode

The fast reaction of the bridge sensor input is achieved through AFE1, which runs at low resolution (10 bit) and highest update rate. AFE2 runs on high resolution (SM+/SM- sequencer, 16bit) and a slower update rate according to Table 39. Figure 32 illustrates the sequence of AFE1 and AFE2 measurements.

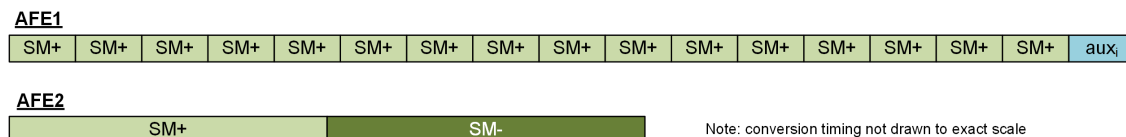


Figure 32: Sequencer Illustration for AFE1 and AFE2

Table 39: ADC Configuration Parameters for Dual Speed Mode

ADC Resolution [Bits]	Full Scale Input Voltage V_{fs} [V]	LSB Size V_{LSB} [μ V]	Conversion Time, Typical, T_{Conv} [μ s]	Conversion Rate, Typical, F_{Conv} [kHz]
10	± 1.418	2768.638	32.54	30.73
16	± 1.440	43.958	887.44	1.13

A digital algorithm decides whether the SSC conditioned results of AFE1 or AFE2 are forwarded to the outputs. By default, the more precise data of AFE2 is forwarded. As soon as a significant signal step occurs at the bridge sensor inputs, the algorithm switches from the slower AFE2 to the fast AFE1. After the transition to AFE1, the outputs follow the AFE1 results with its speed, accuracy, and noise properties.

AFE1 stays active for at least the duration of approximately two slow AFE2 conversions. If no further significant input signal variation is detected within this time, the algorithm switches back from AFE1 to AFE2. See Figure 33 for a graphical explanation of the algorithm.

An input step is detected if the signal difference between AFE1 and AFE2 crosses Threshold 1 (can be setup via GUI Configure\AFE\Sequencer\Dual Speed AFE with AOUT). Once an input step was detected and outputs were switched to AFE1, a count down timer is started to let AFE1 process a number of approximately 60 samples. The actual sample number is between 57 and 61, depending on the configured AFE2 bridge settling time and is automatically calculated by the GUI. Once the count down timer expired, the outputs are switched back from AFE1 to AFE2 if no further step was detected.

To judge the signal variation after the initial step detection, all new AFE1 measurement results are compared against an AFE1 reference result that was stored at the preceding threshold crossing. A further step is detected when the

comparison difference is larger than Threshold 2 (can also be setup via GUI). In this case a new AFE1 reference value is stored and the count down timer is reset which causes another approximately 60 samples from AFE1.

The algorithm detects signal changes which span over multiple AFE1 conversions see Figure 33, it compares the current measurement result with a reference value from several conversion periods back in time. The user can modify the dynamic behavior of the algorithm by modifying the Threshold 1 and Threshold 2 settings.

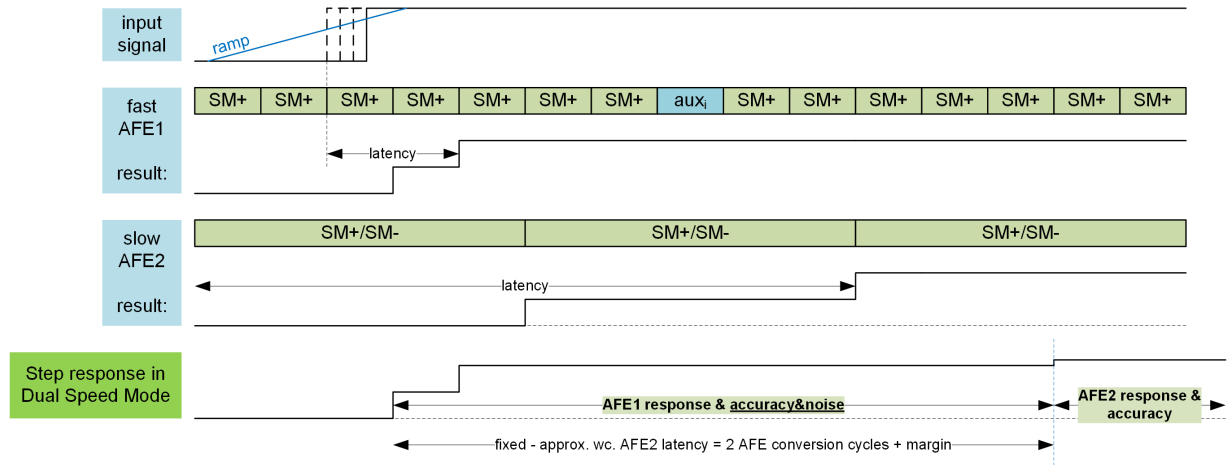


Figure 33: Step Response in Dual Speed Mode for a Significant Single Input Step

The AFE Dual Speed Mode is available for following SSC outputs:

- all Analog Output (AOUT) Modes with exception of 2-wire current loop mode
- all Serial interface outputs

AFE Dual Speed Mode is not available for:

- 2-wire current loop operation
- PMW/FOUT output modes
- Signal Post processing features: EOC, ALARM, Output Filtering.
- AFE diagnosis features

The dynamic Sensor Bridge configuration is fixed to:

- AFE1: 10bit, SM+ only
- AFE2: 16bit, SM+/SM-
- The aux_i cycle in the sequencer becomes automatically activated if T1 or PTAT are selected. If no temperature sensor is selected, the aux_i cycle shown in Figure 32 is removed.

With the dynamic AFE configuration setup a worst case input step latency of 0.35ms is achievable at AOUT. The precise signal settles maximum 5ms after stable input signal.

4.9 Capacitive Sensors - CVC Mode

4.9.1 Capacitive Application Mode 1: Single Ended / Fully Isolated

In Capacitive Application Mode 1, a fully isolated, single-ended measurement of a single capacitive cell is performed.

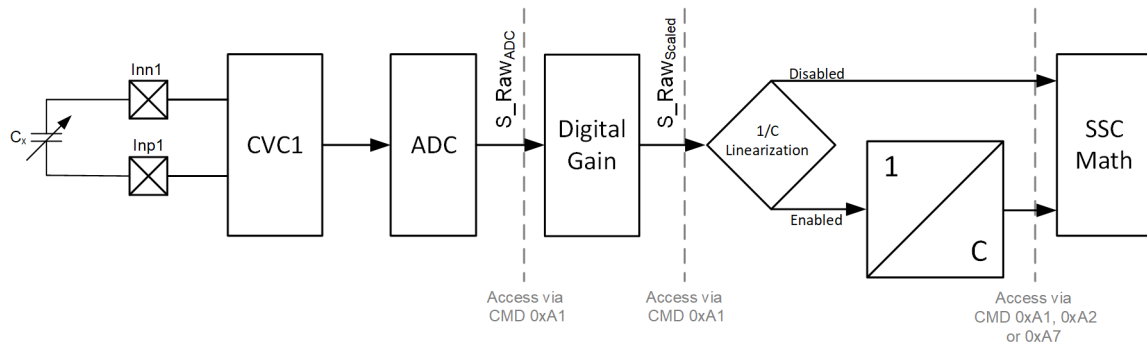


Figure 34: Capacitive Application Mode 1

The Capacitance-to-Voltage Converter (CVC) establishes a ratio between the measured capacitance C_x and an internally selected reference capacitance C_{int} , as shown in Equation 1. Before signal integration, an offset correction can be applied using a capacitance shift value C_{shift} . The adjusted signal is then passed to the ADC for digitization.

$$CVC1 = \frac{(C_x - C_{shift})}{C_{int}} \quad (1)$$

The ADC output is scaled according Equation 2 to amplify low-level input signals. Signal inversion is then applied (Equation 3) to produce a linearized output that corresponds directly to the physical sensor input (for example pressure).

$$S_RawScaled = CVC1 \times Gain_{ADC} \times Gain_{Dig} \quad (2)$$

When 1/C linearization is enabled, the physical signal range must be adjusted using a range shift value R (Equation 4). This compensation accounts for external stray capacitances C_{stray} introduced during sensor module assembly. Accurate characterization of C_{stray} is critical for effective 1/C linearization.

$$S_Raw = \begin{cases} 1/C \text{ Linearization Enabled,} & \frac{1-R^2}{S_RawScaled+R} + R \\ 1/C \text{ Linearization Disabled,} & S_RawScaled \end{cases} \quad (3)$$

$$R = \frac{C_{shift} - C_{stray}}{C_{int}} \times Gain_{ADC} \times Gain_{Dig} \quad (4)$$

Table 40: Capacitive Application Mode 1 Options

Available Options	Values	Comments
C_{int}	20pF to 82pF	Step size 2pF
C_{shift}	0pF to 62pF	Step size 2pF
ADC 2xGain ($Gain_{ADC}$)	Enable/Disable	If "Enable" applies a gain of 2
Digital Gain ($Gain_{Dig}$)	1 to 8	Step size 0.25
1/C Linearization	Enable/Disable	
Range Shift Value (R)	0 to 30	Only available when 1/C Linearization is enabled
Max Input Cap [pF]	<40, <80	With this value, the GUI changes the AFE speed reduction according Table 22
AFE Speed Reduction	1x, 2x, 4x	This value updates automatically when Max Input Cap changes. Check the Override box to enable manual adjustment.

4.9.2 Capacitive Application Mode 2: Single Ended + External Reference / Fully Isolated

In Capacitive Application Mode 2, a single-ended measurement is performed using an external reference capacitance C_r .

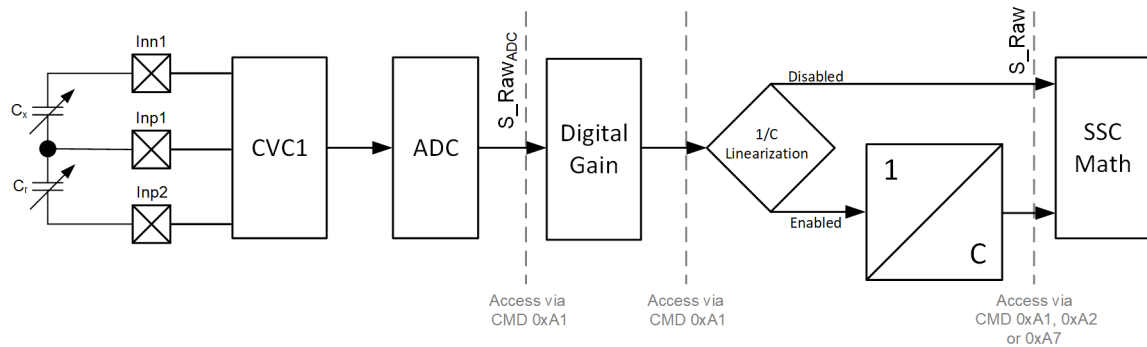


Figure 35: Capacitive Application Mode 2

The CVC calculates the ratio between the measured capacitance C_x and the external reference C_r , as shown in Equation 5. Before the quantitative relation between C_x / C_r is measured, a capacitance shift C_{shift} can be applied to minimize the offset in the measurement signal. The adjusted signal is forwarded to the ADC for digitization.

$$CVC1 = CVC_{out} = \frac{C_x - C_{shift}}{C_r} \quad (5)$$

The digitized output is scaled according to Equation 6, enabling effective use of low input signal levels. Optional signal inversion can be applied, as illustrated in Equation 7, resulting in a linear output that accurately reflects changes in the physical input quantity.

$$S_Raw_{Scaled} = CVC1 \times Gain_{ADC} \times Gain_{Dig} \quad (6)$$

If 1/C linearization is enabled, the signal inversion must also be applied to the physical signal range. This requires shifting the scaled signal S_Raw_{Scaled} by a range shift value R , as defined in Equation 8. The range shift value R accounts for the external stray capacitances C_{stray} , which are introduced during sensor module assembly. Accurate consideration of C_{stray} significantly enhances the effectiveness of the 1/C linearization.

$$S_Raw = \begin{cases} 1/CLinearizationEnabled, & \frac{1-R^2}{S_Raw_{Scaled}+R} + R \\ 1/CLinearizationDisabled, & S_Raw_{Scaled} \end{cases} \quad (7)$$

$$R = \frac{C_{shift} - C_{stray}}{mean(C_r)} \times Gain_{ADC} \times Gain_{Dig} \quad (8)$$

Table 41: Capacitive Application Mode 2 Options

Available Options	Values	Comments
C_{shift}	0pF to 62pF	Step size 2pF
ADC 2xGain ($Gain_{ADC}$)	Enable/Disable	If "Enable" applies a gain of 2
Digital Gain ($Gain_{Dig}$)	1 to 8	Step size 0.25
1/C Linearization	Enable/Disable	
Range Shift Value (R)	0 to 30	Only available when 1/C Linearization is enabled
Max Input Cap [pF]	<40, <80	With this value, the GUI changes the AFE speed reduction according Table 22
AFE Speed Reduction	1x, 2x, 4x	This value updates automatically when Max Input Cap changes. Check the Override box to enable manual adjustment.

4.9.3 Capacitive Application Mode 3: Differential / Fully Isolated

In Capacitive Application Mode 3, a differential measurement of two isolated capacitive sensors (C_x and C_y) is performed.

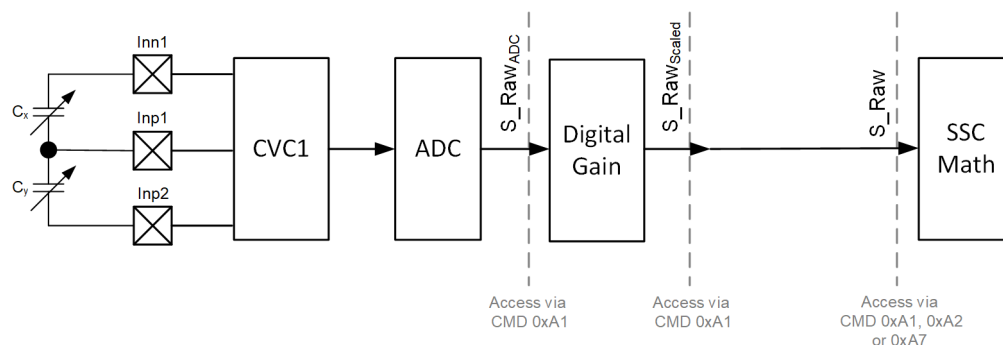


Figure 36: Capacitive Application Mode 3

The CVC calculates the difference between C_x , C_y , and the reference C_{int} , as shown in Equation 9. Before the reference capacitor integrates the signal, a capacitance shift C_{shift} can be applied to reduce offset in the measurement. The adjusted signal is forwarded to the ADC for digitization.

Note: For optimal operation, C_x should be greater than C_y . If no pressure is applied and this is not the case, swap the sensor connections.

$$CVC1 = \frac{C_x - C_y - C_{shift}}{C_{int}} \quad (9)$$

The resulting signal is scaled using Equation 10, effectively amplifying the measurement so that low input signal spans can be utilized.

$$S_Raw_{Scaled} = S_Raw = (CVC1 \times Gain_{ADC} - \frac{AdcShift}{8}) \times Gain_{Dig} \quad (10)$$

Table 42: Capacitive Application Mode 3 Options

Available Options	Values	Comments
C_{int}	20pF to 82pF	Step size 2pF
C_{shift}	0pF to 62pF	Step size 2pF
ADC 2xGain ($Gain_{ADC}$)	Enable/Disable	If "Enable" applies a gain of 2
ADCShift	0 to 0.875	Step size 0.125
Digital Gain ($Gain_{Dig}$)	1 to 8	Step size 0.25
Max Input Cap [pF]	<40, <80	With this value, the GUI changes the AFE speed reduction according Table 22
AFE Speed Reduction	1x, 2x, 4x	This value updates automatically when Max Input Cap changes. Check the Override box to enable manual adjustment.

4.9.4 Capacitive Application Mode 4: Single ended / Referred to Ground

In Capacitive Application Mode 4, a single-ended measurement is performed on a capacitive sensor C_x that is connected to ground.

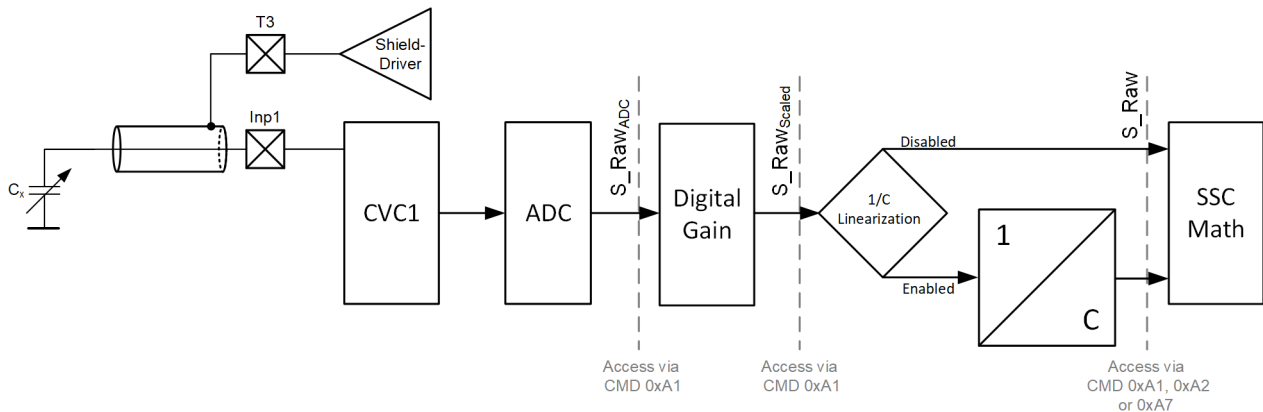


Figure 37: Capacitive Application Mode 4

The capacitance-to-voltage converter (CVC) calculates the ratio between C_x and an internally selected reference capacitance C_{int} , as shown in Equation 11. Before the reference capacitor integrates the signal, a capacitance shift C_{shift} can be applied to reduce offset in the measurement. The adjusted signal is forwarded to the ADC for digitization.

$$CVC1 = \frac{C_x - C_{shift}}{C_{int}} \quad (11)$$

The signal from the ADC is scaled according to Equation 2, effectively amplifying the measurement so that low input signal spans can be utilized. Afterward, signal inversion is applied, as shown in Equation 3, resulting in a linear output that accurately reflects changes in the physical input quantity.

$$S_Raw_{Scaled} = CVC1 \times Gain_{ADC} \times Gain_{Dig} \quad (12)$$

If 1/C linearization is enabled, the signal inversion must also be applied to the physical signal range. This requires shifting the scaled signal S_Raw_{Scaled} by a range shift value R , as defined in Equation 14. The range shift value R accounts for the external stray capacitances C_{stray} , which are introduced during sensor module assembly. Accurate consideration of C_{stray} significantly enhances the effectiveness of the 1/C linearization.

$$S_Raw = \begin{cases} 1/C \text{ Linearization Enabled,} & \frac{1-R^2}{S_Raw_{Scaled}+R} + R \\ 1/C \text{ Linearization Disabled,} & S_Raw_{Scaled} \end{cases} \quad (13)$$

$$R = \frac{C_{shift} - C_{stray}}{C_{int}} \times Gain_{ADC} \times Gain_{Dig} \quad (14)$$

Table 43: Capacitive Application Mode 4 Options

Available Options	Values	Comments
C_{int}	20pF to 82pF	Step size 2pF
C_{shift}	0pF to 62pF	Step size 2pF
ADC 2xGain ($Gain_{ADC}$)	Enable/Disable	If "Enable" applies a gain of 2
Digital Gain ($Gain_{Dig}$)	1 to 8	Step size 0.25
1/C Linearization	Enable/Disable	
Range Shift Value (R)	0 to 30	Only available when 1/C Linearization is enabled
$CM1EnShieldDrv$	Enable/Disable	Enables a 1nF ShieldDriver
$CMShieldDrv10nF$	Enable/Disable	Enables a 10nF instead of 1nF ShieldDriver Only available if $CM1EnShieldDrv$ or/and $CM2EnShieldDrv$ is activated
Max Input Cap [pF]	<50, <100	With this value, the GUI changes the AFE speed reduction according Table 23
AFE Speed Reduction	1x, 2x, 4x	This value updates automatically when Max Input Cap changes. Check the Override box to enable manual adjustment.

4.9.5 Capacitive Application Mode 5: Single ended + External Reference / Referred to Ground

In Capacitive Application Mode 5, a single-ended measurement is performed using an external reference capacitor C_r , with both measurement and reference nodes connected to ground.

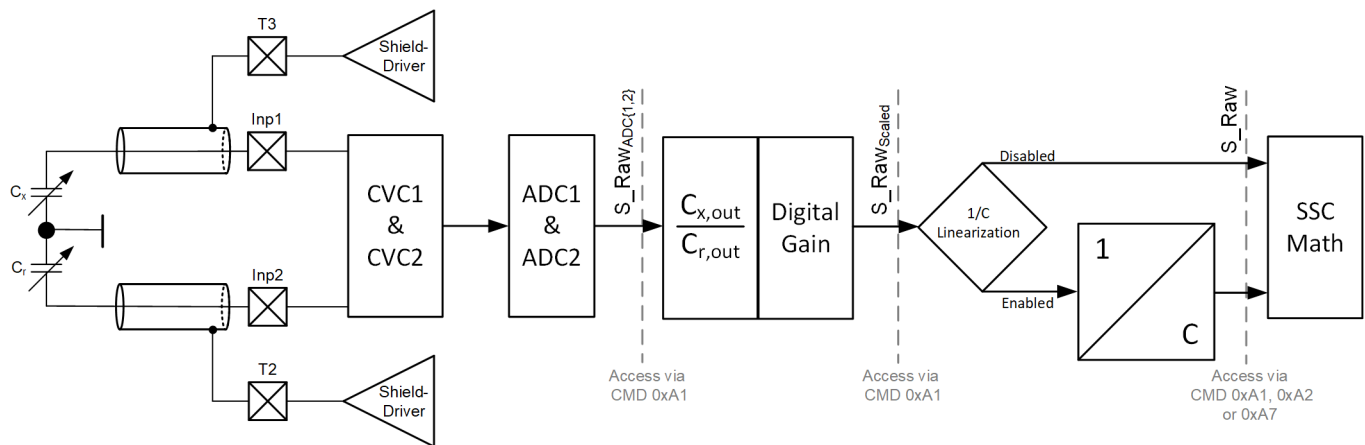


Figure 38: Capacitive Application Mode 5

The capacitance-to-voltage converter (CVC) establishes a ratio between the measured capacitance C_x and reference capacitance C_{int} , as shown in Equation 15, also a ratio between the measured capacitance C_r and an internally selected reference capacitance C_{int} , as shown in Equation 16. Before the reference capacitor integrates the signals, a capacitance shift C_{shift} can be applied to reduce offset in the measurement. The adjusted signal is then forwarded to the ADC for digitization.

$$CVC1 = \frac{C_x - C_{shift}}{C_{int}} \quad (15)$$

$$CVC2 = \frac{C_r - C_{shift}}{C_{int}} \quad (16)$$

Note: C_{int} and C_{shift} have the same value for both measurements.

The analog signals can be increased in the ADC as shown in Equation 17 and Equation 18, effectively amplifying the measurement so that low input signal spans can be utilized.

$$S_{rawAdc1} = CVC1 \times Gain_{ADC} \quad (17)$$

$$S_{rawAdc2} = CVC2 \times Gain_{ADC} \quad (18)$$

Once digitized, the ratio between the input and reference signal is computed and scaled, shown in the Equation 19. After determination an digital gain can be applied.

$$S_Raw_{Scaled} = \frac{S_Raw_{Adc1}}{S_Raw_{Adc2} + \frac{C_{shift}}{C_{int}} \times Gain_{ADC}} \times Gain_{Dig} \quad (19)$$

The Equation 19 can be simplified, shown in Equation 20.

$$S_Raw_{Scaled} = \frac{C_x - C_{shift}}{C_r} \times Gain_{Dig} \quad (20)$$

If 1/C linearization is enabled, the signal inversion must also be applied to the physical signal range. This requires shifting the scaled signal S_Raw_{Scaled} by a range shift value R, as defined in Equation 22. The range shift value R accounts for the external stray capacitances C_{stray} , which are introduced during sensor module assembly. Accurate consideration of C_{stray} significantly enhances the effectiveness of the 1/C linearization.

$$S_Raw = \begin{cases} 1/C \text{ Linearization Enabled,} & \frac{1-R^2}{S_Raw_{Scaled}+R} + R \\ 1/C \text{ Linearization Disabled,} & S_Raw_{Scaled} \end{cases} \quad (21)$$

$$R = \frac{C_{shift} - C_{stray}}{mean(C_r)} \times Gain_{Dig} \quad (22)$$

Table 44: Capacitive Application Mode 5 Options

Available Options	Values	Comments
C _{int} AFE1/2	20pF to 82pF	Step size 2pF
C _{shift} AFE1/2	0pF to 62pF	Step size 2pF
ADC 2xGain (Gain _{ADC})	Enable/Disable	If "Enable" applies a gain of 2
Digital Gain (Gain _{Dig})	1 to 8	Step size 0.25
1/C Linearization	Enable/Disable	
Range Shift Value (R)	0 to 30	Only available when 1/C Linearization is enabled
Cm1EnShieldDrv	Enable/Disable	Enables a 1nF ShieldDriver
Cm2EnShieldDrv	Enable/Disable	Enables a 1nF ShieldDriver
CmShieldDrv10nF	Enable/Disable	Enables a 10nF instead of 1nF ShieldDriver Only available if CM1EnShieldDrv or/and CM2EnShieldDrv is activated
Max Input Cap [pF]	<50, <100	With this value, the GUI changes the AFE speed reduction according Table 23
AFE Speed Reduction	1x, 2x, 4x	This value updates automatically when Max Input Cap changes. Check the Override box to enable manual adjustment.

4.9.6 Capacitive Application Mode 6: Differential / Referred to Ground

In Capacitive Application Mode 6, a differential measurement is performed between two grounded capacitive sensors C_x and C_y .

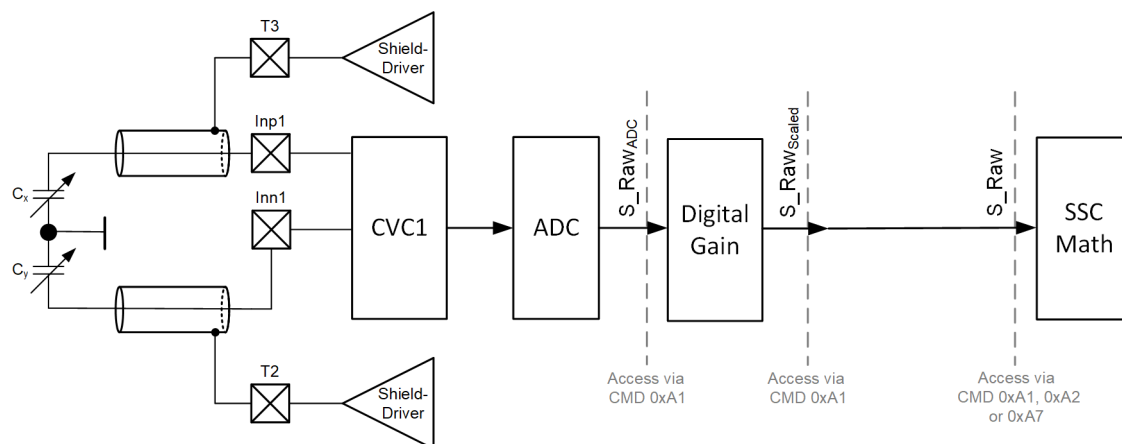


Figure 39: Capacitive Application Mode 6

The CVC calculates the difference between C_x , C_y , and the reference C_{int} , as shown in Equation 23. Before the reference capacitor integrates the signal, a capacitance shift C_{shift} can be applied to reduce offset in the measurement. The adjusted signal is forwarded to the ADC for digitization.

Note: For optimal operation, C_x should be greater than C_y . If no pressure is applied and this is not the case, swap the sensor connections.

$$CVC1 = \frac{C_x - C_y - C_{shift}}{C_{int}} \quad (23)$$

The signal from the ADC is scaled according to Equation 24, effectively amplifying the measurement so that low input signal spans can be utilized.

$$S_{RawScaled} = S_{Raw} = (CVC1 \times Gain_{ADC} - \frac{AdcShift}{8}) \times Gain_{Dig} \quad (24)$$

Table 45: Capacitive Application Mode 6 Options

Available Options	Values	Comments
C_{int}	20pF to 82pF	Step size 2pF
C_{shift}	0pF to 62pF	Step size 2pf
ADC 2xGain ($Gain_{ADC}$)	Enable/Disable	If "Enable" applies a gain of 2
ADCShift	0 to 0.875	Step size 0.125
Digital Gain ($Gain_{Dig}$)	1 to 8	Step size 0.25
Cm1EnShieldDrv	Enable/Disable	Enables a 1nF ShieldDriver
Cm2EnShieldDrv	Enable/Disable	Enables a 1nF ShieldDriver
CmShieldDrv10nF	Enable/Disable	Enables a 10nF instead of 1nF ShieldDriver Only available if CM1EnShieldDrv or/and CM2EnShieldDrv is activated
Max Input Cap [pF]	<50, <100	With this value, the GUI changes the AFE speed reduction according Table 23
AFE Speed Reduction	1x, 2x, 4x	This value updates automatically when Max Input Cap changes. Check the Override box to enable manual adjustment.

4.9.7 Capacitive Application Mode 11: Differential $(C_x - C_y)/(C_x + C_y)$ / Referred to Ground

In Capacitive Application Mode 11, a differential ratio of two grounded capacitive sensors C_x and C_y is measured and processed for linearization.

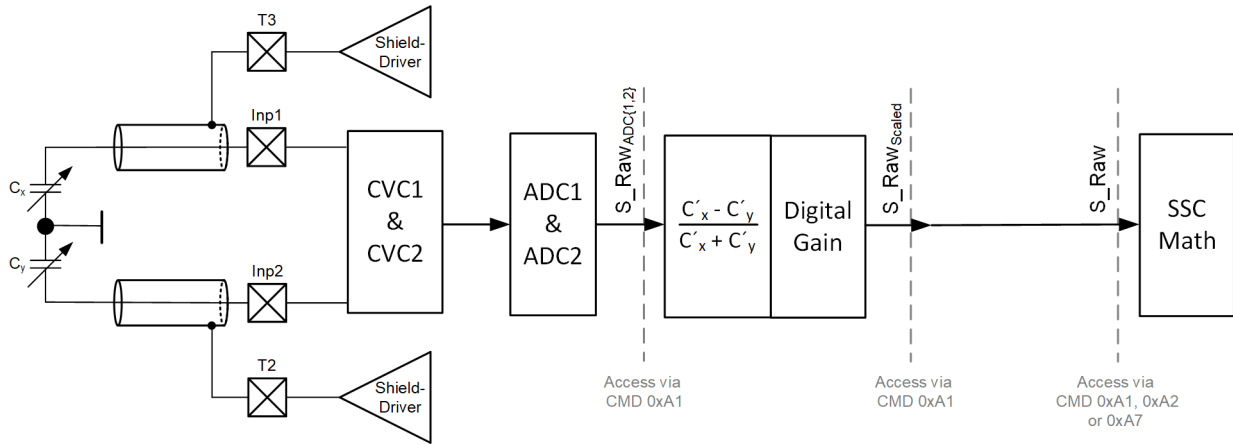


Figure 40: Capacitive Application Mode 11

The CVC calculates a ratio between the measured capacitance C_x and an internally selected reference capacitance C_{int} , as shown in Equation 25, and also a ratio between the measured capacitance C_y and an internally selected reference capacitance C_{int} , as shown in Equation 26. Before the reference capacitor integrates the signals, a capacitance shift C_{shift} can be applied to reduce offset in the measurement. The adjusted signal is forwarded to the ADC for digitization.

$$CVC1 = \frac{C_x - C_{shift1}}{C_{int}} \quad (25)$$

$$CVC2 = \frac{C_y - C_{shift2}}{C_{int}} \quad (26)$$

Note: C_{int} has the same value for both measurements, to ensure a common base.

The analog signals can be amplified by the ADC gain stage as shown in Equation 27 and Equation 28.

$$S_Raw_{Adc1} = CVC1 \times Gain_{ADC} \quad (27)$$

$$S_Raw_{Adc2} = CVC2 \times Gain_{ADC} \quad (28)$$

After digitization of both signals, the pure ratio $(C_x - C_y)/(C_x + C_y)$ is obtained by compensating with the range shift value R , as shown in Equation 29. This compensation accounts for the average of the capacitance shift values C_{shift1} , C_{shift2} , the internal reference capacitance C_{int} , and the external stray capacitance C_{stray} , which is introduced during sensor module assembly.

$$S_Raw_{Scaled} = S_Raw = \frac{S_Raw_{Adc1} - S_Raw_{Adc2}}{S_Raw_{Adc1} + S_Raw_{Adc2} + 2 \times R} \times Gain_{Dig} \quad (29)$$

$$R = \frac{mean(C_{shift1,2}) - C_{stray}}{C_{int}} \times Gain_{ADC} \quad (30)$$

Table 46: Capacitive Application Mode 11 Options

Available Options	Values	Comments
C _{int} AFE1/2	20pF to 82pf	Step size 2pf
C _{shift1} AFE1	0pF to 62pf	Step size 2pf
C _{shift2} AFE2	0pF to 62pf	Step size 2pf
ADC 2xGain (Gain _{ADC})	Enable/Disable	If "Enable" applies a gain of 2
Digital Gain (Gain _{Dig})	1 to 31	Step size 0.25
Range Shift Value (R)	0 to 10	Only available when 1/C Linearization is enabled
Cm1EnShieldDrv	Enable/Disable	Enables a 1nF ShieldDriver
Cm2EnShieldDrv	Enable/Disable	Enables a 1nF ShieldDriver
CmShieldDrv10nF	Enable/Disable	Enables a 10nF instead of 1nF ShieldDriver Only available if CM1EnShieldDrv or/and CM2EnShieldDrv is activated
Max Input Cap [pF]	<50, <100	With this value, the GUI changes the AFE speed reduction according Table 23
AFE Speed Reduction	1x, 2x, 4x	This value updates automatically when Max Input Cap changes. Check the Override box to enable manual adjustment.

5 Sensor Signal Conditioning

5.1 Signal Conditioning Data Path

Figure 41 illustrates the sensor signal conditioning flow that is applied for AFE output data to compensate for offset, gain, non-linearity, and temperature effects and to calculate the conditioned data for further output processing. See subsection 5.2 to subsection 5.6 for more information on the basis mathematical subfunctions.

The signal path from conditioned data to individual output signals is described in section 6.

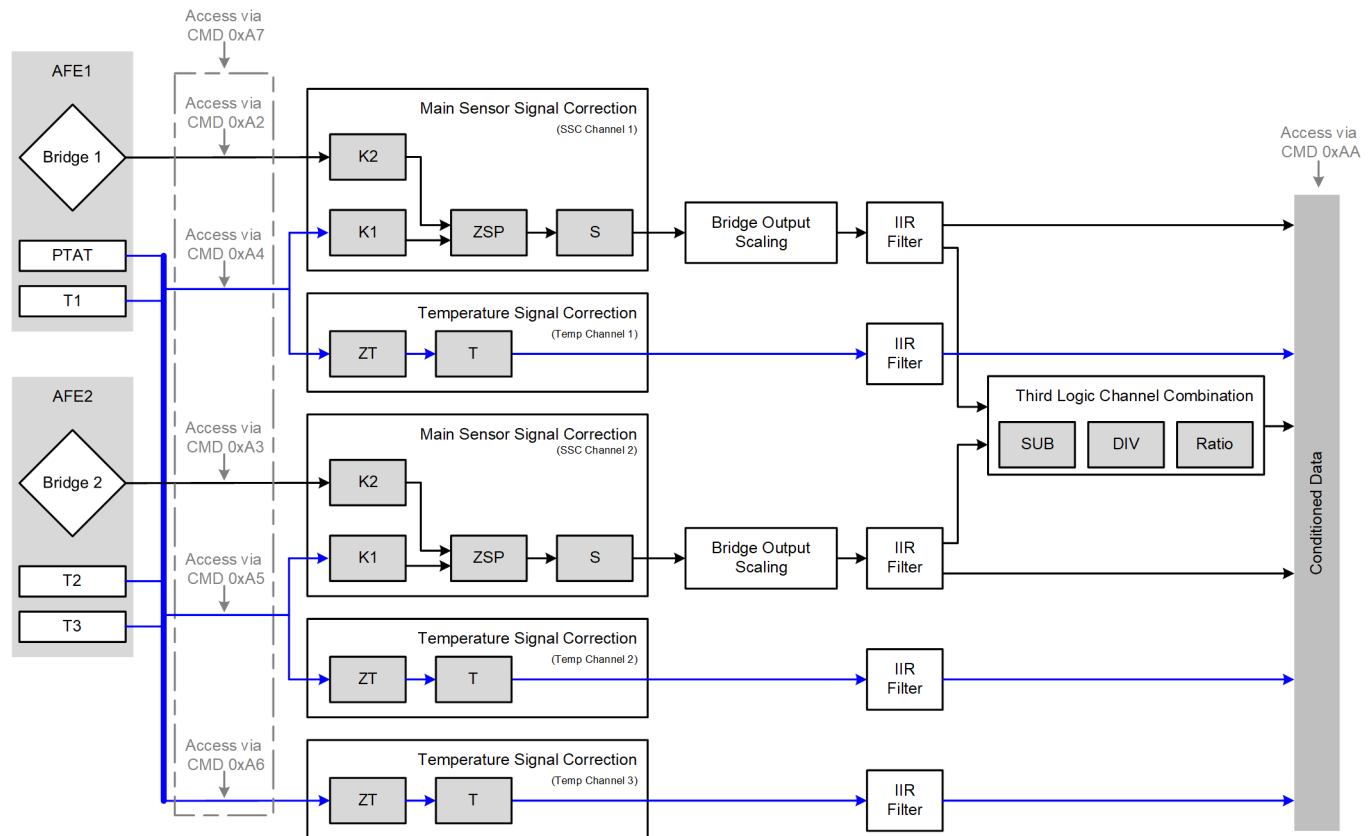


Figure 41: Sensor Signal Flow Chart from Input to Conditioned Data

5.2 Main Sensor Signal Correction

ZSSC3281 supports basic second-order compensation of sensor nonlinearities. The following basic SSC math options are available:

- Sensor signal correction
 - SOT Curve-0: Parabolic compensation curve
 - SOT Curve-1: S-shaped compensation curve
- Temperature signal correction

The parabolic compensation is recommended for most sensor types. The applied SSC math option can be selected in the GUI through the field Calibration\Curve.

The available SSC capabilities for SOT Curve-0 and SOT Curve-1 are described in Table 47, Table 48, and Table 49. The used equation terms are as follows:

		Valid Input Range
S	Corrected sensor reading output via I2C, OWI, or SPI	0x0 to 0xFFFFF
S_Raw	Raw sensor reading from ADC (after AZ correction, depends on Afe1SmConfig)	-(0x7FFFFF) to 0x7FFFFF
$Gain_S$	Sensor gain term	-(0x7FFFFF) to 0x7FFFFF
$Offset_S$	Sensor offset term	-(0x7FFFFF) to 0x7FFFFF
Tcg	Temperature coefficient gain term	-(0x7FFFFF) to 0x7FFFFF
Tco	Temperature coefficient offset term	-(0x7FFFFF) to 0x7FFFFF
T_Raw	Raw temperature reading (after AZ correction)	-(0x7FFFFF) to 0x7FFFFF
SOT_tcg	Second-order term for Tcg non-linearity	-(0x7FFFFF) to 0x7FFFFF
SOT_tco	Second-order term for Tco non-linearity	-(0x7FFFFF) to 0x7FFFFF
SOT_sens	Second-order term for sensor non-linearity	-(0x7FFFFF) to 0x7FFFFF
$SENS_shift$	Post-calibration, post-assembly offset shift	-(0x7FFFFF) to 0x7FFFFF
$... $	Absolute value	
$[...]_{ll}^{ul}$	Bound/saturation number range from ll to ul , overflow and/or underflow is reported as saturation in the Status Byte	

All raw data and compensation coefficients supplied to the formulas are required in 24-bit data format shown in Table 47 and Table 48.

Table 47: Data Format of Raw ADC Readings

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	-2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 48: Data Format of 24-bit SSC Coefficients

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	0 = positive 1 = negative	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

The compensated result data is supplied in 24-bit data format as shown in Table 49.

Table 49: Data Format of Corrected SSC Results (S and T)

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

5.2.1 Pre-calculation

Simplified:

$$K_1 = 2^{23} + \frac{T_Raw}{2^{23}} \times \left(\frac{4 \times SOT_tcg}{2^{23}} \times T_Raw + 4 \times Tcg \right) \quad (31)$$

$$K_2 = 4 \times Offset_S + S_Raw + \frac{T_Raw}{2^{23}} \times \left(\frac{4 \times SOT_tco}{2^{23}} \times T_Raw + 4 \times Tco \right) \quad (32)$$

Complete:

$$K_1 = \left[2^{23} + \left[\frac{T_Raw}{2^{23}} \times \left[\left[\frac{SOT_tcg}{2^{21}} \times T_Raw \right]_{-2^{25}}^{2^{25}-1} + 4 \times Tcg \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \quad (33)$$

$$K_2 = \left[4 \times Offset_S + \left[S_Raw + \left[\frac{T_Raw}{2^{23}} \times \left[\left[\frac{SOT_tco}{2^{21}} \times T_Raw \right]_{-2^{25}}^{2^{25}-1} + 4 \times Tco \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \quad (34)$$

5.2.2 SOT Curve-0 (Parabolic Compensation)

Simplified:

$$Z_{SP} = \frac{4 \times Gain_S}{2^{23}} \times \frac{K_1}{2^{23}} \times K_2 + 2^{23} \quad (35)$$

$$S = \frac{Z_{SP}}{2^{23}} \times \left(\frac{4 \times SOT_sens}{2^{23}} \times Z_{SP} + 2^{23} \right) + SENS_shift \quad (36)$$

Note: Z_{SP} and S are delimited to positive number range.

Complete:

$$Z_{SP} = \left[\left[\frac{Gain_S}{2^{21}} \times \left[\frac{K_1}{2^{23}} \times K_2 \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_0^{2^{25}-1} \quad (37)$$

$$S = \left[\left[\frac{Z_{SP}}{2^{23}} \times \left[\left[\frac{SOT_sens}{2^{21}} \times Z_{SP} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + SENS_shift \right]_0^{2^{24}-1} \quad (38)$$

5.2.3 SOT Curve-1 (S-shaped Compensation)

Simplified:

$$Z_{SS} = \frac{4 \times Gain_S}{2^{23}} \times \frac{K_1}{2^{23}} \times K_2 \quad (39)$$

Note: K_1 and K_2 according to Equation 33 and Equation 34.

$$S = \frac{Z_{SS}}{2^{23}} \times \left(\frac{4 \times SOT_sens}{2^{23}} \times |Z_{SS}| + 2^{23} \right) + 2^{23} + SENS_shift \quad (40)$$

Note: S is delimited to positive number range.

Complete:

$$Z_{SS} = \left[\frac{Gain_S}{2^{21}} \times \left[\frac{K_1}{2^{23}} \times K_2 \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \quad (41)$$

$$S = \left[\left[\left[\frac{Z_{SS}}{2^{23}} \times \left[\left[\frac{SOT_sens}{2^{21}} \times |Z_{SS}| \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} + SENS_shift \right]_0^{2^{24}-1} \quad (42)$$

5.3 Temperature Signal Correction

Temperature is measured either internally by the ZSSC3281, through an additional external element, or by means of a combination of ZSSC3281 internal and external temperature sensing capabilities. Temperature correction contains both linear gain and offset terms as well as a second-order term to correct for any nonlinearities. For temperature, second-order compensation is always parabolic.

The correction equation terms are as follows:

		Valid Input Range
T	Corrected temperature sensor reading output via digital interface	0x0 to 0xFFFFF
T_Raw	Raw temperature reading after AZ correction	-(0x7FFFFF) to 0x7FFFFF
$Gain_T$	Gain coefficient for temperature	-(0x7FFFFF) to 0x7FFFFF
$Offset_T$	Offset coefficient for temperature	-(0x7FFFFF) to 0x7FFFFF
SOT_T	Second-order term for temperature source nonlinearity	-(0x7FFFFF) to 0x7FFFFF
T_shift	Shift for post-calibration/post-assembly offset compensation	-(0x7FFFFF) to 0x7FFFFF

The correction formula is best represented as a two-step process as follows:

Simplified:

$$Z_T = \frac{4 \times Gain_T}{2^{23}} \times (T_Raw + 4 \times Offset_T) + 2^{23} \quad (43)$$

$$T = \frac{Z_T}{2^{23}} \times \left(\frac{4 \times SOT_T}{2^{23}} \times Z_T + 2^{23} \right) \quad (44)$$

Note: Z_T and T are delimited to positive number range.

Complete:

$$Z_T = \left[\left[\frac{Gain_T}{2^{21}} \times [T_Raw + 4 \times Offset_T]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_0^{2^{25}-1} \quad (45)$$

$$T = \left[\left[\frac{Z_T}{2^{23}} \times \left[\left[\frac{SOT_T}{2^{21}} \times Z_T \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + T_shift \right]_0^{2^{24}-1} \quad (46)$$

5.4 Bridge Output Scaling

ZSSC3281 offers a linear rescaling function to amplify or compress a partial region of the sensor input range to the desired signal output range. Figure 42 illustrates the rescaling on an example where the 25% to 75% calibrated signal input range is mapped to the output range of 0% to 100%. The feature is intended for customers who need to separate product derivatives after a common sensor calibration step.

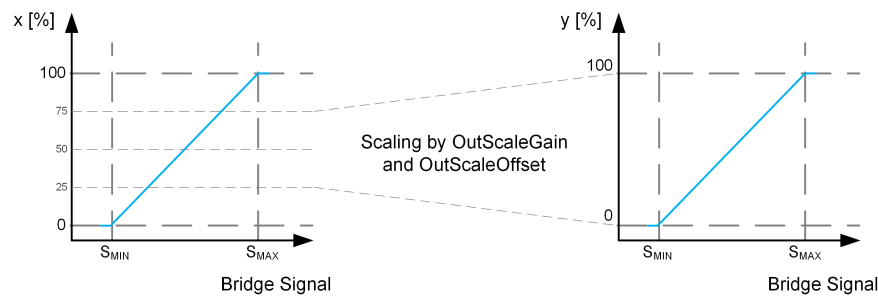


Figure 42: Example: Bridge Output Scaling Function for Scaling 25% - 75%, to final 0% - 100%

The rescaling feature applies the following formula to the SSC conditioned outputs of the main bridge sensor:

$$S_{Scaled} = \left[\frac{8 \times OutScaleGain}{2^{23}} \times (S + 8 \times OutScaleOffset) \right]_{0}^{2^{24}-1} \tag{47}$$

The Coefficients *OutScaleGain* and *OutScaleOffset* are stored in the CCP (Configuration and Calibration Page) of ZSSC3281 in signed magnitude format. According to Table 50 *OutScaleGain* is limited to a maximum gain of 4 and the *OutScaleOffset* can vary from -1.5 to 0 related to the SSC result number range 0 to ~2.

Table 50: Examples for Bridge Output Scaling

Input Relative – x [%]		OutScaleGain		OutScaleOffset		Output Relative – y [%]	
		real	CCP Content (Decimal)	real	CCP Content (Decimal)		
0	50.0	2.000	2097152	0.0	0	0	100
0	33.3	3.003	3148876	0.0	0	0	100
0	25.0	4.000	4194304	0.0	0	0	100
25	50.0	4.000	4194304	-0.5	-524288	0	100
25	75.0	2.000	2097152	-0.5	-524288	0	100
50	100.0	2.000	2097152	-1.0	-1048576	0	100
75	100.0	4.000	4194304	-1.5	-1572864	0	100

Table 51 lists the mapping of CCP register content to output scaling coefficients.

Table 51: Data Format of Output Scaling Coefficients in CCP

Bit Number	23	22	21	20	19	...	1	0
Meaning, Weighting	0 = positive 1 = negative	2 ²	2 ¹	2 ⁰	2 ⁻¹	...	2 ⁻¹⁹	2 ⁻²⁰

The GUI supports the calculation of *OutScaleGain* and *OutScaleOffset* based on provided relative input and output range specifications (can be configured on the GUI tab Configure\Output Scaling).

5.5 IIR Filter

The conditioned outputs of the two main sensor bridge channels CH1 and CH2 and the conditioned outputs of the temperature channels TCh1 to TCh3 can be low pass filtered for noise reduction. Each channel is equipped with an independent configurable IIR Filter. The mathematical filter description is as follows:

$$IIR_{Out(0)} = S_{Scaled(0)} \quad (48)$$

$$IIR_{Out(i)} = S_{Scaled(i-1)} + \frac{(S_{Scaled(i)} - IIR_{Out(i-1)}) \times Diff}{Avg} \quad (49)$$

where:

$$Diff = FiltDiff + 1 \quad (50)$$

$$Avg = 2^{FiltAvg} \quad (51)$$

FiltDiff and *FiltAvg* represent the filter coefficients which are stored as unsigned 3-bit values per filter channel in *IirFiltCoeffReg* inside the CCP of ZSSC3281. They are determined by the GUI (Configure\Filter) depending on the filter Tau selections made by the user. For a stable system, the $Diff \leq Avg$ must be ensured.

The filter Tau can be calculated by:

$$\frac{Diff}{Avg} = \alpha \approx \frac{1}{\tau_{dig}} = \frac{\Delta T}{\tau_{ana}} \quad (52)$$

$$\tau_{dig} = -\frac{1}{\ln(1 - \alpha)} \quad (53)$$

τ_{dig} is given in number of digital samples.

5.6 Third Logic Channel Combination

The potentially pre-scaled and filtered two main sensor bridge channels Ch1 and Ch2 of ZSSC3281 can be mathematically combined to calculate the output of a third logic channel Ch3. Channel Ch3 is only available in the synchronized AFE mode which is enabled via the GUI menu Configure\AFE\Sequencer\AFE Selection and Configurability\selection: "AFE1+AFE2, config equally".

The calculation result on Ch3 is available through serial interface read out only. The digital output format is signed 32-bit (two's complement), see Table 52. Outputting the Ch3 result at AOUT is possible for subtraction and ratio only. Division is readable via digital interfaces only.

The Third Logic Channel (TLC) can be configured via the GUI menu Configure\TLC menu.

Following mathematical operations are available:

- Subtraction: (Ch1 – Ch2) or (Ch2 – Ch1)
- Division: (Ch1 / Ch2) or (Ch2 / Ch1)
- Ratio: If $IIR_{Out_Ch1} == IIR_{Out_Ch2}$ then $IIR_{Out_Ch3} = 1$
 Else if $IIR_{Out_Ch1} < IIR_{Out_Ch2}$ then $IIR_{Out_Ch3} = IIR_{Out_Ch1} / IIR_{Out_Ch2}$
 Else $IIR_{Out_Ch3} = 2 - (IIR_{Out_Ch2} / IIR_{Out_Ch1})$

Note: Division calculation can lead to math saturation, which is not suppressed by firmware.

Calibration of the sensor channels Ch1 and Ch2 must still be done independently applying the single channel calibration routines.

Table 52: Data Format of Logic Output Channel Ch3 at Serial Interface

Bit Number	31	30	29	...	24	23	22	21	...	2	1	0
Meaning, Weighting	-2^8	2^7	2^6	...	2^1	2^0	2^{-1}	2^{-2}	...	2^{-21}	2^{-22}	2^{-23}

6 Post Processing Options for Conditioned Sensor Signals

6.1 Signal Post Processing Flow Chart

Figure 43 illustrates the signal flow from conditioned data to individual output signals. All basis mathematical sub-functions are described within the subsection 6.5 to subsection 6.6.

The signal path from AFE output data to conditioned data is described in subsection 5.2.

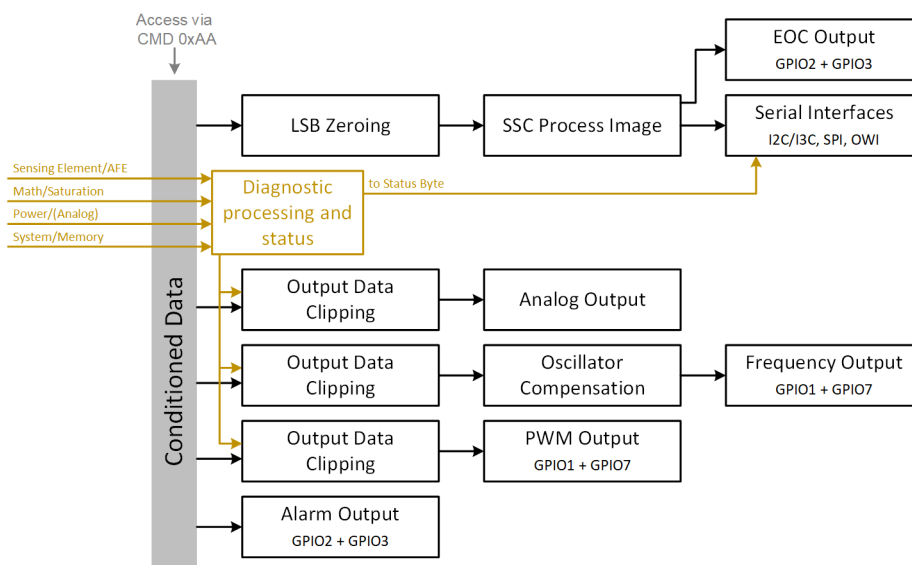


Figure 43: Sensor Signal Flow Chart from Input to Output

6.2 LSB Zeroing

All internal calculations are performed with higher precision than the selected ADC resolution, and the output results on digital interfaces are normalized for all channels except SSC CH3 (Third Logic Channel) before providing on the digital interfaces as defined by:

$$\text{DigitalOutputValue} = \text{ConditionedData} \text{ AND } (2^{\text{ADCResolution}} - 1) \quad (54)$$

6.3 SSC Process Image

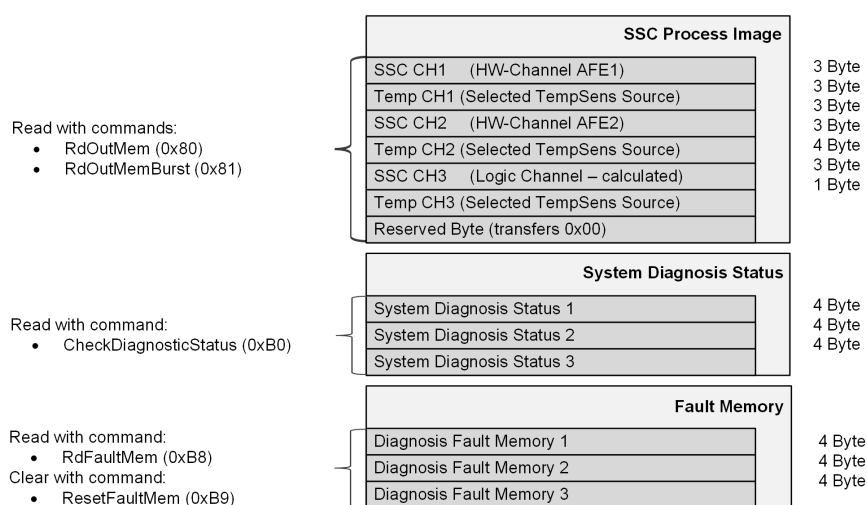


Figure 44: SSC Process Image, System Diagnosis Status and Fault Memory Map

ZSSC3281 handles all continuous process data communication with a host system through memory interfaces called SSC Process Image, System Diagnosis Status, and Fault Memory.

The data in the SSC Process Image is updated as soon as respective AFE measurements are completed, and the related sensor signal conditioning operations are carried out. It always reflects the most up-to-date known status of the connected sensor system. The SSC Process Image holds data of both main sensor, three temperature signals and for the third logic channel.

Status informations from all activated system diagnosis checks are contained inside the System Diagnosis Status and the Fault Memory which allows the host system to check for the source of system failure states that were reported in the Status Byte of a previously received command response. The structure of the system diagnosis status words is described in subsection 7.2.

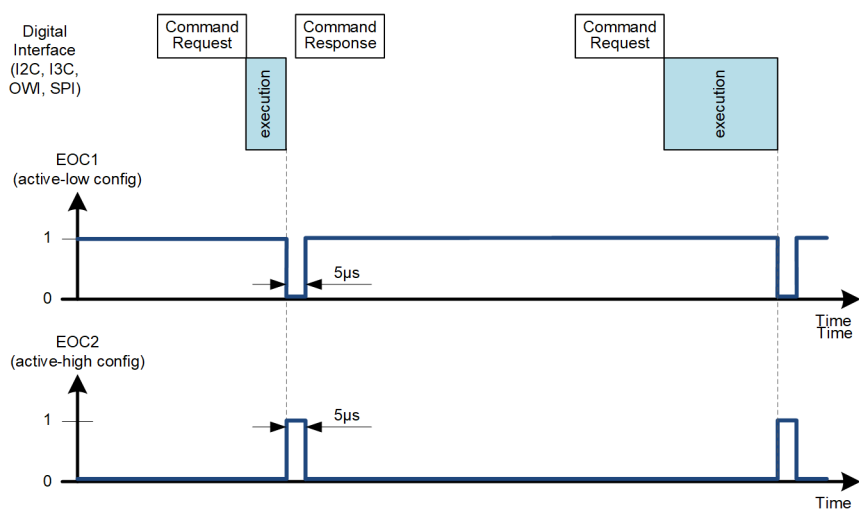
6.4 EOB/EOC/Alarm Functions

The Pins EOC/ALARM 1 (GPIO2) and EOC/ALARM 2 (GPIO3) can be configured to operate either as an end-of-busy (EOB) in Command and Sleep Mode, or end-of-conversion (EOC) transducer or as a configurable switch/alarm transducer for the respective SSC conditioned outputs of the main bridge sensors in Cyclic Mode.

To support different external logic, the global setting for polarity of the EOB/EOC/ALARM outputs can be configured as active high or active low (can be setup via GUI Configure\EOC/ALARM\Output Polarity).

6.4.1 EOB Function

The end-of-busy (EOB) function can be enabled as an additional functionality within Command Mode and Sleep Mode (setup via GUI Configure\System Control) to allow upper MCUs receiving interrupt signals after finishing ZSSC3281's internal command execution. If EOB is enabled, a short signal pulse of approximately 5µs wide (see Figure 45) is generated on enabled EOC pins.



Note: timing relations are not to scale, they are qualitative illustrations only

Figure 45: EOB Behavior - Signalization of End-of-Busy

6.4.2 EOC Function

If the EOC output mode is active (can be setup via GUI Configure\EOC\ALARM\Selected Mode\EOC), an EOC event is signaled at the GPIO pin as soon as a new SSC-corrected measurement result of the bridge sensor is available for read out by the host system. The EOC signal pulse is approximately 5µs wide (see Figure 46).

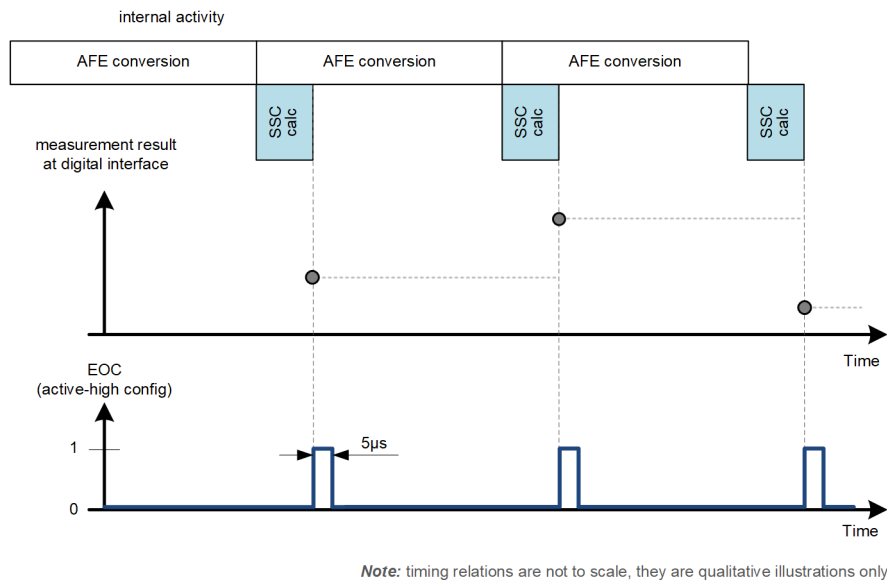


Figure 46: EOC Behavior - Signalization of End-of-Conversion

Note: The EOC Output Mode is not available in AFE Dual Speed Mode PWM/FOUT Mode

6.4.3 ALARM Function

If the ALARM output mode is active (can be setup via GUI Configure\EOC\ALARM\Selected Mode\Alarm) further configuration options exist:

- Single threshold comparison vs. Window comparison
- Range definition for ALARM (above/below vs. inside/outside)
- Hysteresis setting
- Persistence setting

Figure 47 shows the ALARM output signaling in the possible four different modes. The dotted black lines reflect the behavior for zero hysteresis, while the dotted blue lines take a configured threshold hysteresis into account.

The lower charts of Figure 47 feature a special signal transient example. If the measurement result jumps from one sample to another from above the upper to below the lower alarm threshold (or vice versa), the alarm state remains the same since the logic conditions of the Window comparison mode permit this.

The configured hysteresis value (GUI tab Configure\EOC\ALARM\Hysteresis) defines the hysteresis half width or “offset”. The total hysteresis width is effectively twice the configured hysteresis value.

The ALARM persistence can be set between 0 and 255. A persistence value >0 requires the signal to remain above or below the threshold for the selected number of consecutive pulses before the ALARM output state is changed. The value of 0 effectively disables the persistence feature and the logic checks for a single occurrence of the threshold condition only.

If AFE1 and AFE2 are running asynchronously, the EOC/ALARM outputs are also evaluated independently after the SSC operation was completed. In case of synchronous setup, the evaluations happen at about the same time but AFE1 is evaluated first.

The alarm thresholds and hysteresis values are stored in the respective CCP registers using the data format as shown in Table 53.

Table 53: Data Format of Alarm Thresholds and Hysteresis

Bit-Number:	23	22	21	20	...	2	1	0
Meaning, Weighting	20	2^1	2^2	2^3	...	2^{21}	2^{22}	2^{23}

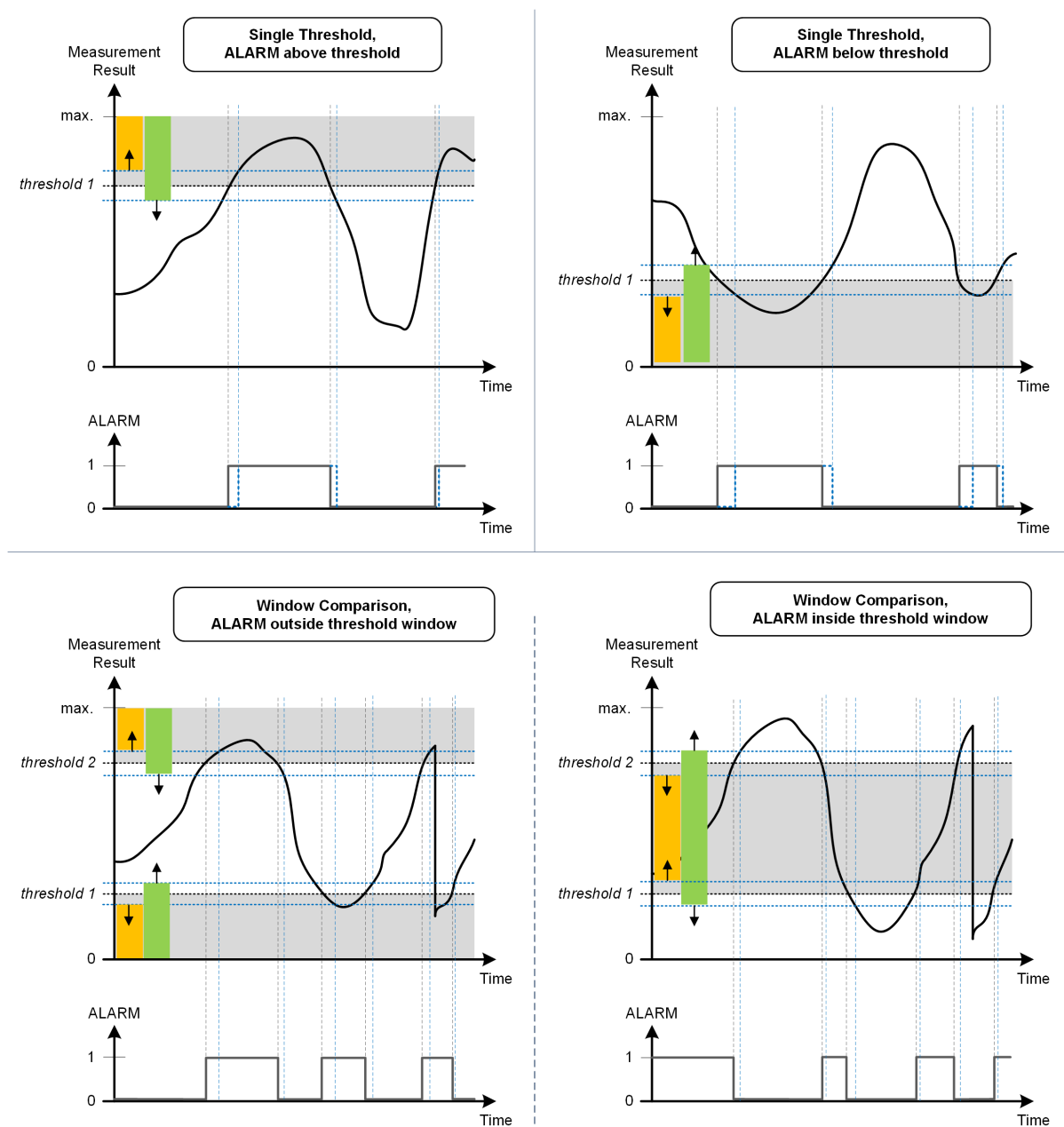


Figure 47: Behaviour of ALARM Feature in Four Different Modes

6.5 Output Data Clipping

The signaling of a diagnosis failure state can also be activated on the analog output AOUT via the GUI tab Diagnostic\General. If the signalization of Diagnostic State at AOUT is enabled, discovered diagnostic failure states can be either mapped to the Upper or the Lower Diagnostic Range (UDR and LDR) of the output span (GUI tab Diagnostic\Sensor\AFE).

The boundaries of the upper and lower diagnostic ranges are configurable via the GUI tab Configure\Output Pre-process. They are typically set to 5% and 95% of the full scale output level but can be modified to the application needs.

To prevent false interpretation of very large or very low output signals, the conditioned data is clipped according to Figure 48 to fit into the remaining output range between UDR and LDR before it is forwarded to the AOUT output.

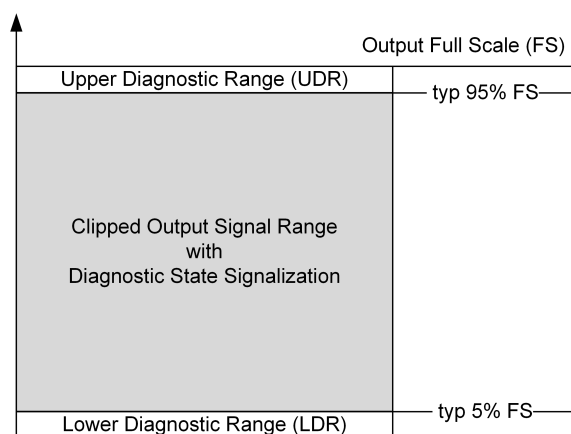


Figure 48: AOUT Output Ranges with Active Diagnostic State Signalization

- Note:** There is no rescaling of the conditioned data performed at this stage.
If rescaling of the conditioned data to the clipped output signal range is required, use the Bridge Output Scaling feature (see subsection 5.4) or use different target values during the SSC calibration process.
- Note:** UDR has higher priority than LDR.
Each sensor and AFE diagnostic feature described in subsection 7.1 assigns individually UDR or LDR which requires an internal prioritization in case of multiple malfunctions detected.

6.6 FOUT Oscillator Compensation

Frequency output requires a stable base frequency. The internal oscillator provides the base frequency for frequency modulation (see subsection 9.1). To minimize the resulting temperature drift, it can be compensated via internal PTAT temperature sensor by the following compensation mathematics:

<i>FOUT</i>	Corrected sensor signal selected for Frequency Output
<i>OutputDataClipping</i>	Temperature compensated output signal for Frequency Output
<i>T_{RawPTAT}</i>	Raw temperature reading of PTAT (after AZ correction)
<i>Fm_{SOT}</i>	Second-order term for frequency modulation
<i>Fm_{Gain}</i>	Gain term for frequency modulation
<i>Fm_{Offset}</i>	Offset term for frequency modulation

Valid Input Range
0x0 to 0xFFFFFFFF
0x0 to 0xFFFFFFFF
-(0x7FFFFFFF) to 0x7FFFFFFF
-(0x7FFFFFFF) to 0x7FFFFFFF
-(0x7FFFFFFF) to 0x7FFFFFFF
-(0x7FFFFFFF) to 0x7FFFFFFF

- Note:** The compensation mathematics requires enabling the internal PTAT temperature measurement within the AUX measurements.

All raw data and compensation coefficients supplied to the formulas are required in the 24-bit data format described in Table 21, Table 22, Table 23, and Equation 25.

Table 54: Data Format of Raw ADC Readings

Bit-Number:	23	22	21	20	...	2	1	0
Meaning, Weighting	2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 55: Data Format of Corrected SSC Result

Bit-Number:	23	22	21	20	...	2	1	0
Meaning, Weighting	2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 56: Data Format of 32-bit SSC Coefficients

Bit-Number:	23	22	21	20	...	2	1	0
Meaning, Weighting	2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-28}	2^{-29}	2^{-30}

$$FOUT = [OutputDataClipping \times (4 \times Fm_{SOT} \times T_{RawPTAT}^2 + Fm_{Gain} \times T_{RawPtat} + Fm_{Offset})]_0^{2^{32}-1} \quad (55)$$

7 Sensor and System Diagnosis

The ZSSC3281 sensor and system diagnosis function can detect several false conditions on externally connected sensors and monitor long term gain and offset drifts of the analog front end. This makes ZSSC3281 well suited for sensing applications that require increased system reliability as well as for predictive maintenance supervision done by the host system.

7.1 Sensor and AFE Diagnostic Features

The supported sensor and AFE diagnostic features are summarized in Table 57.

Table 57: Sensor and AFE Diagnosis Functions

Monitored Input or Component	Failure Category	Failure Condition ¹
Main sensor (resistive sensor bridge 1)	INP or INN open	INP to INN resistance >125kΩ
	INP or INN shorted	INP to INN resistance <170Ω
Main sensor (resistive sensor bridge 2)	INP or INN open	INP to INN resistance >125kΩ
	INP or INN shorted	INP to INN resistance <170Ω
Temperature sensor T1	Short to Top (TOP)	T1 to TOP resistance <500Ω
	Short to Bottom (BOT)	T1 to BOT resistance <500Ω
	Open	T1 resistance >2MΩ, 500kΩ, 100kΩ
Temperature sensor T2	Short to Top (TOP)	T2 to TOP resistance <500Ω
	Short to Bottom (BOT)	T2 to BOT resistance <500Ω
	Open	T2 resistance >2MΩ, 500kΩ, 100kΩ
Temperature sensor T3	Short to Top (TOP)	T3 to TOP resistance <500Ω
	Short to Bottom (BOT)	T3 to BOT resistance <500Ω
	Open	T3 resistance >2MΩ, 500kΩ, 100kΩ
AFE1 (resistive and capacitive sensor)	Gain Drift	Gain check deviates by provided percentage from previously stored reference value
	Offset Drift	Offset check deviates by provided permillage from previously stored reference value
AFE2 (resistive and capacitive sensor)	Gain Drift	Gain check deviates by provided percentage from previously stored reference value
	Offset Drift	Offset check deviates by provided permillage from previously stored reference value
CVC1 (capacitive sensor)	Leakage 1	Leakage measurement exceeds the defined tolerance
	Leakage 2	Leakage measurement exceeds the defined tolerance
CVC2 (capacitive sensor)	Leakage 1	Leakage measurement exceeds the defined tolerance
	Leakage 2	Leakage measurement exceeds the defined tolerance

¹ Typical values. Further specifications are provided in subsection 2.4.

For all active sensor inputs and AFEs, the checks can be enabled selectively on the GUI tab Diagnostic\Sensor\AFE.

The AFE gain drift check (for resistive sensor bridges) employs an internally connected resistive DAC to create itself a defined input signal. The internal DAC can generate four different input voltages: 2mV, 10mV, 100mV, 200mV. The GUI proposes the most suitable setting based on other configurations made for the AFE. The selected voltage level is stored in the CCP.

In order to make proper use of the long-term AFE gain and offset drift checks, a device dependent reference value must be acquired and stored during the sensor calibration process. The GUI supports this via the 'Get' button which is located in front of the GainRef and OffsetRef fields.

To run individual tests for sensor and AFE diagnosis features, use the 0xB4 command. This command triggers a single measurement that returns a pass or fail result, as shown in Table 58. A full update of all enabled sensor checks can be executed using the 0xB2 command.

Table 58: 0xB4 - Self Diagnostic Measurement Command

Command Code	Description	Return
0xB4 followed by 0x0XY	Self-Diagnostic Measure for AFE1 and AFE2 <ul style="list-style-type: none"> 0x0X <ul style="list-style-type: none"> AFE1: 0x00 AFE2: 0x01 0xY - see below 	2 Bytes
0xY	Measurement	Return
0x05	External temperature sensor T1, check short to top	0b0000_0000_0000_000X
0x06	External temperature sensor T1, check short to bottom	0b0000_0000_0000_000X
0x07	External temperature sensor T1, check open	0b0000_0000_0000_000X
0x0A	External temperature sensor T2, check short to top	0b0000_0000_0000_000X
0x0B	External temperature sensor T2, check short to bottom	0b0000_0000_0000_000X
0x0C	External temperature sensor T2, check open	0b0000_0000_0000_000X
0x0F	External temperature sensor T3, check short to top	0b0000_0000_0000_000X
0x10	External temperature sensor T3, check short to bottom	0b0000_0000_0000_000X
0x11	External temperature sensor T3, check open	0b0000_0000_0000_000X
0x1B	Main sensor (resistive sensors) connection check open	0b0000_0000_0000_000X
0x1C	Main sensor (resistive sensors) connection check short	0b0000_0000_0000_000X
0x27	AFE offset drift (resistive and capacitive sensor)	0b0000_0000_0000_000X
0x28	AFE gain drift (resistive and capacitive sensor)	0b0000_0000_0000_000X
0x29	CVC Leakage 1 (capacitive)	0b0000_0000_0000_000X
0x2A	CVC Leakage 2 (capacitive)	0b0000_0000_0000_000X

7.2 Sensor and System Diagnosis Status

All individual sensor and AFE diagnosis features are able to set an individual bit inside a fault memory.

Since the SSC Process Image data is continuously updated as soon as new measurement data becomes available, it may happen that diagnosis faults disappear before the host has read them via the CheckDiagnosticStatus command 0xB0.

To allow system failure detection at a later point in time, ZSSC3281 additionally stores all appeared system diagnosis failures in a separate volatile fault memory. The fault memory has the same organization as the system Diagnosis Status Memory and becomes cleared only via ClearFaultMem (0xB9) command or a system reset. The fault memory can be read via RdFaultMem (0xB8) command.

Reading the fault memory or diagnosis status memory returns three words as shown in Table 59, Table 60, and Table 61. The complete fault memory or diagnosis status memory can be updated using the 0xB2 command.

Diagnoses detailed in Table 59 and Table 60 trigger the sensor fault bit within the status byte.

Similarly, diagnoses described in Table 61 set the saturation bit within the status byte.

The status byte is fully described in subsection 10.1.1.

Table 59: Fault Memory - Word 0 - Bits 31:0

Bits	Description	Bits	Description
31 : 25	Reserved	16	AFE1 temperature sensor broken connection check T1 open: $R > R_{T_OPEN}$
24	AFE2 temperature sensor shorted connection check T3 to BOT shorted: $R < R_{T_SHORT}$	15 : 9	Reserved
23	AFE2 temperature sensor shorted connection check T3 to TOP shorted: $R < R_{T_SHORT}$	8	AFE2 sensor shorted connection check → INP2 – INN2 shorted: $R < R_{short}$
22	AFE2 temperature sensor broken connection check T3 open: $R > R_{T_OPEN}$	7	AFE2 sensor broken connection check → INP2 or INN2 open: $R > R_{broken}$
21	AFE2 temperature sensor shorted connection check T2 to BOT shorted: $R < R_{T_SHORT}$	6 : 3	Reserved
20	AFE2 temperature sensor shorted connection check T2 to TOP shorted: $R < R_{T_SHORT}$	2	AFE1 sensor shorted connection check → INP1 – INN1 shorted: $R < R_{short}$
19	AFE2 temperature sensor broken connection check T2 open: $R > R_{T_OPEN}$	1	AFE1 sensor broken connection check → INP1 or INN1 open: $R > R_{open}$
18	AFE1 temperature sensor shorted connection check T1 to BOT shorted: $R < R_{T_SHORT}$	0	Reserved
17	AFE1 temperature sensor shorted connection check T1 to TOP shorted: $R < R_{T_SHORT}$		

Table 60: Fault Memory - Word 1 - Bits 31:0

Bits	Description
31 : 8	Reserved
7	CVC2 leakage 2
6	CVC2 leakage 1
5	CVC1 leakage 2
4	CVC1 leakage 1
3	AFE2 Offset Drift (resistive and capacitive sensor)
2	AFE2 Gain Drift (resistive and capacitive sensor)
1	AFE1 Offset Drift (resistive and capacitive sensor)
0	AFE1 Gain Drift (resistive and capacitive sensor)

Table 61: Fault Memory - Word 2 - Bits 31:0

Bits	Description
31 : 6	Reserved
5	SSC calculation unit OR raw output data saturation channel 3, temperature sensor data
4	SSC calculation unit channel 3, bridge sensor data
3	SSC calculation unit OR raw output data saturation channel 2, temperature sensor data
2	SSC calculation unit OR raw output data saturation channel 2, bridge sensor data
1	SSC calculation unit OR raw output data saturation channel 1, temperature sensor data
0	SSC calculation unit OR raw output data saturation channel 1, bridge sensor data

8 Analog Output

The conditioned and post processed output data of one of the following channels can be made available as analog output signal at the Analog Output AOOUT

- Bridge Sensor Channel 1
- Bridge Sensor Channel 2
- Third Logic Channel
- Temperature Channel 1
- Temperature Channel 2
- Temperature Channel 3

Depending on the configuration of the Analog Output Driver, two different output modes, (absolute voltage output and current mode output) are supported.

8.1 Analog Output Driver

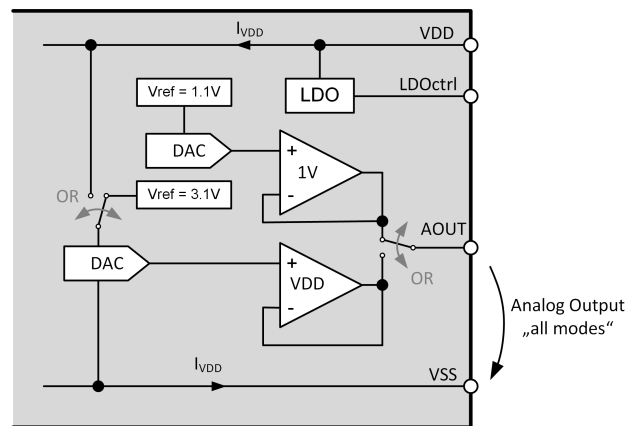


Figure 49: Block Schematic AOUT Driver

The Analog Output Driver contains two separate output buffers, one for a full-scale voltage of 1V and another one for full scale voltages ranging up to VDD. The following functional assignments apply:

- 1V buffer
 - 1V absolute Voltage Mode
 - 2-wire current loop mode
 - 3-wire current loop mode
- VDD buffer
 - Ratiometric Voltage Mode
 - 3V absolute Voltage Mode
 - 5V absolute Voltage Mode
 - 10V absolute Voltage Mode

The VDD buffer offers a programmable output current limiting function which is not available for the 1V buffer. The VDD buffer requires the VDD to be in the range between 2.7V and 5.5V for proper operation.

8.2 Negative Voltage Generation for AOUT

To support True-0V signals on the Analog Output (AOUT), ZSSC3281 provides an option to externally supply a negative voltage rail for the AOUT buffer at VDDN. VDDN supply specifications are shown in Table 62. The external circuitry must ensure to not generate a VDDN voltage of less than -0.5V to prevent latchup conditions for the internal circuitry.

The negative VDDN voltage can also be generated by an internal charge pump circuit. The internal charge pump can be activated through GUI field: Configure\AOUT\VDDN Charge Pump. The field Configure\AOUT\VDDN Load allows to set a maximum current that the internal charge pump can supply.

The activation of the internal charge pump at VDDN considerably increases the power consumption of ZSSC3281 and needs to be carefully considered in applications where current consumption of the sensor device (sensor + ZSSC3281) is a critical parameter. The VDDN charge pump can only be used for $VDD \geq 2.7V$.

If no True-0V signals are required at AOUT, the user must disable the VDDN charge pump in the GUI and directly connect VDDN with VSS on PCB level.

The charge pump function is only available for all AOUT Operation Modes with Voltage Output. The charge pump circuit requires an external buffer capacitor C_{VDDN} and a Schottky Diode to work properly.

Table 62: Parameter Negative Voltage for AOUT

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
VDD_{CP}	VDD operating range of internal charge pump		2.7		5.5	V
$VDDN$	Negative voltage supply for analog output (AOUT)	Internally generated, requires activation of VDDN charge pump		$V_{ExtSchottky}$		V
		Externally supplied	0	-0.3V	-0.5V	V
I_{VDDN}	Available charge pump load current	Programmable in 4 steps.			0.5	mA
					1	
					3	
					5	
I_{VDD}	Additional charge pump current consumption at VDD	0.5mA load current	0.5	4.5	5	mA
		1.0mA load current	1	9	10	
		3.0mA load current	3	15.5	17	
		5.0mA load current	5	25	30	
C_{VDDN}	Buffer capacitance at pin VDDN			1		μF
$V_{FW-Schottky}$	Forward voltage of external Schottky diode			0.3	0.5	V

8.3 Analog Output Configuration

8.3.1 Ratiometric Voltage Mode

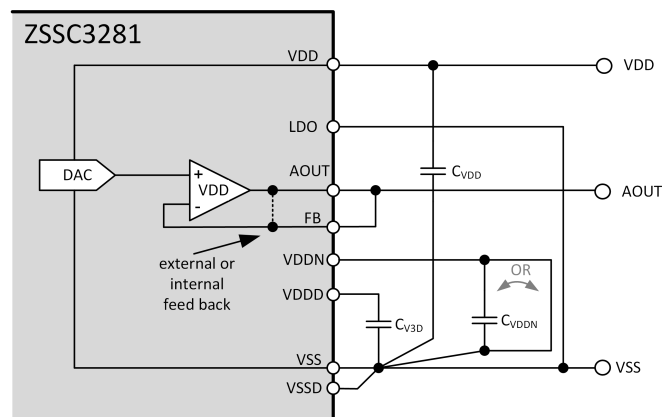


Figure 50: Ratiometric Output Mode Configuration at AOUT

The SSC output can be ratiometric mapped to 0 to VDD range with the application circuit shown in Figure 50 and activation of the Ratiometric Voltage Mode in the GUI via Configure\AOUT\Operation Mode\Ratiometric Voltage. In Ratiometric Output Mode the reference voltage for the AOUT DAC is identical to the VDD level.

8.3.2 5V Absolute Voltage Mode

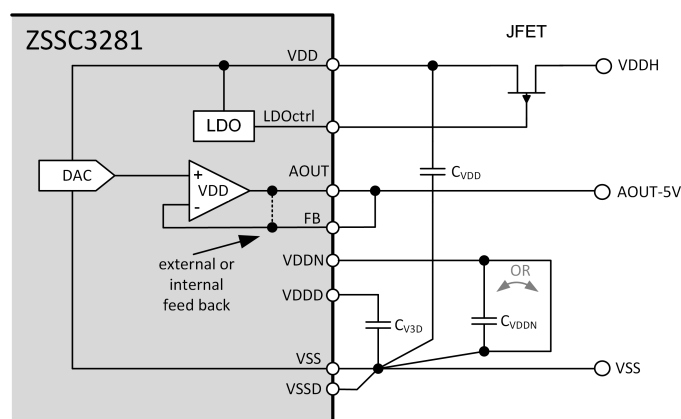


Figure 51: 5V Absolute Output Voltage Configuration at AOUT

The SSC output can be mapped to 0V to 5V voltage range with the application circuit shown in Figure 51 and activation of the 5V Absolute Voltage Mode in the GUI via Configure\AOUT\Operation Mode\Absolute Voltage 0V – 5V. This AOUT mode requires the external regulator supply configuration to be active in the GUI with the regulated VDD set to 5.25V.

The applied reference voltage for the AOUT DAC is directly derived from VDD through a digital factory calibration coefficient.

8.3.3 10V Absolute Voltage Mode

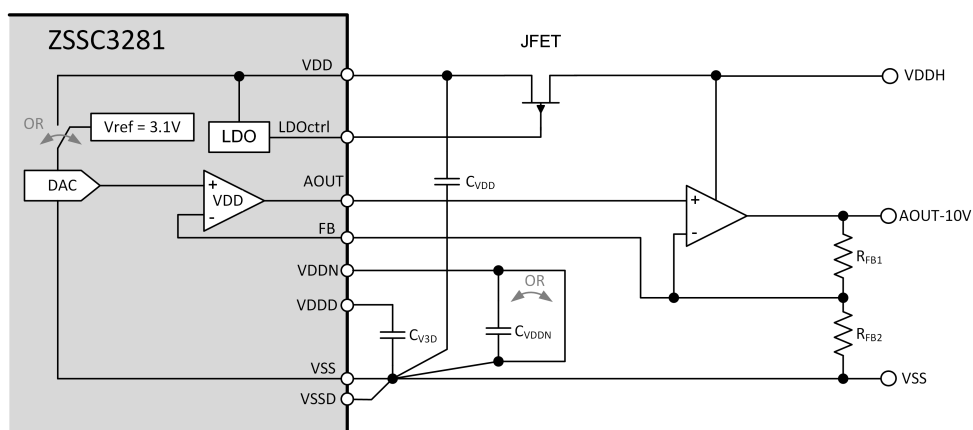


Figure 52: 10V Absolute Output Voltage Configuration at AOUT

The SSC output can be mapped to a 0V to 10V voltage range using the application circuit shown in Figure 52 and activating the 10V Absolute Voltage Mode in the GUI under Configure\AOUT\Operation Mode\Absolute Voltage 0V – 10V. For this mode, the DAC reference can be selected as either the internal 3.1V or VDD reference. When using the VDD reference, this AOUT mode requires the external regulator supply configuration to be active in the GUI, with the regulated VDD set to 5.25V.

The reference voltage applied to the AOUT DAC is directly derived from VDD through a digital factory calibration coefficient. To achieve a 0V to 10V output signal, the VDD or 3.1V absolute voltage output can be scaled to higher voltages using an external operational amplifier. For improved voltage accuracy, connect the Feedback Pin FB to the inverting input of the external operational amplifier that is offset compensated. The calculation for the external voltage amplification factor is as follows:

$$A = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \quad (56)$$

8.3.4 1V Absolute Voltage Mode

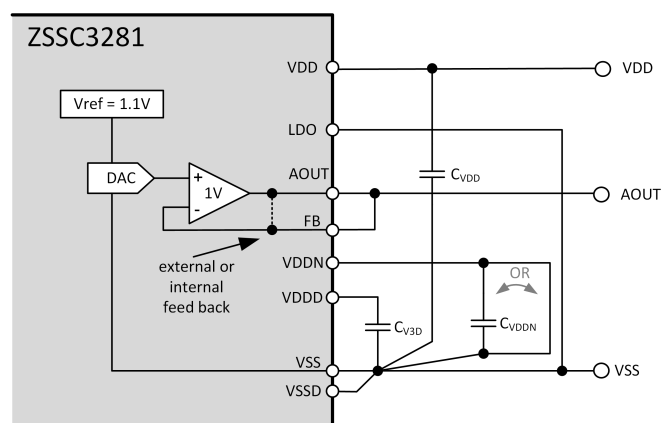


Figure 53: 1V Absolute Output Voltage Configuration at AOUT

The SSC output can be mapped to 0V to 1V voltage range with the application circuit shown in Figure 53 and activation of the 1V Absolute Voltage Mode in the GUI via Configure\AOUT\Operation Mode\Absolute Voltage 0V – 1V. The applied reference voltage for the AOUT DAC is generated from an internal factory calibrated bandgap source.

the default CCP parameters 'CL2_Offset' and 'CL2_Delta' based on the entered R_{sense} (typical value), required and measured I_{min} and I_{max} values. To activate the optimized values, a Write Memory operation needs to be triggered by the user. 'CL2_Offset' and 'CL2_Delta' determine the swing of the AOUT voltage to cover the 4mA to 20mA current output signal.

The user can select the signal which shall be mapped to the 2-Wire Current Loop output via the drop-down menu Configure\AOUT\AOUT Pin Mapping.

8.3.7 3-Wire Current Loop Mode

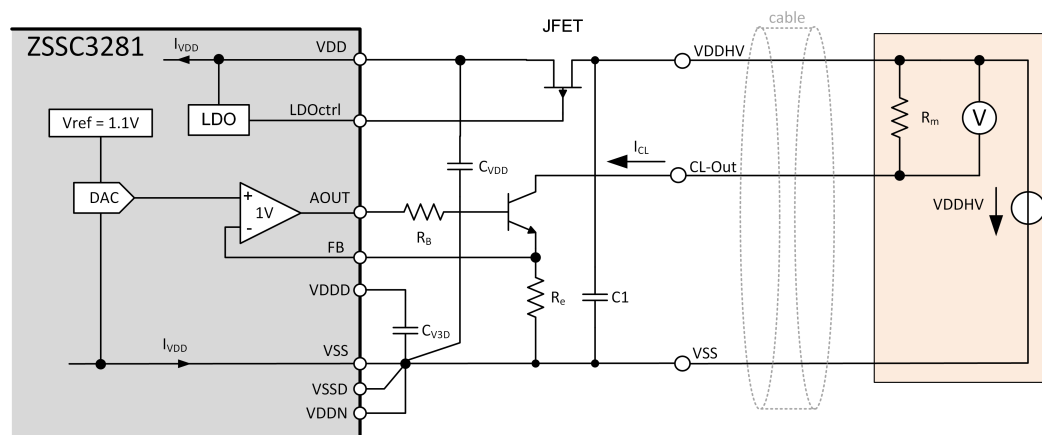


Figure 56: 3-wire NPN Current Loop Configuration at AOUT

Table 64: External Components in 3-Wire Current Loop Mode

Symbol	Parameter	Minimum	Typical	Maximum	Units
R_e	Emitter resistor		43		Ω
R_b	Base resistor		4700		Ω
T_1	Bipolar Transistor	for example BCX56-16			n.a.

The SSC output can be mapped to an input current at CL-Out in the application circuit shown in Figure 56 and by activation of the 3-Wire Current Loop Mode in the GUI via Configure\AOUT\Operation Mode\3-Wire Current Loop.

The signal current at CL-Out is typically required to range from 4mA to 20mA. The available min/max signal current range at CL-Out depends on the actual value of the external emitter resistor R_e .

To compensate for tolerances of R_e , the GUI offers a post calibration option to calibrate the current loop current to the required absolute accuracy. The function recalculates the default CCP parameters 'CL3_Offset' and 'CL3_Delta' based on the entered R_e (typical value), required and measured I_{min} and I_{max} values. To activate the optimized values, a Write Memory operation needs to be triggered by the user. 'CL3_Offset' and 'CL3_Delta' determine the swing of the AOUT voltage to cover the 4mA to 20mA current output signal.

The user can select the signal to map to the 3-Wire Current Loop output via the drop-down menu Configure\AOUT\AOUT Pin Mapping.

9 Digital Outputs/Output Modulation

The conditioned and post processed output data of two of the following channels can be made available as modulated digital output signal at the pins FOUT/PWM_1 (GPIO1) and FOUT/PWM_2 (GPIO7)

- Bridge Sensor Channel 1
- Bridge Sensor Channel 2
- Third Logic Channel
- Temperature Channel 1
- Temperature Channel 2
- Temperature Channel 3

The channel assignment to the output pins and the type of output modulation can be selected in the GUI via Configure\DOUT tab. There will be two types of output modulation supported:

- Frequency Modulation
- Pulse Width Modulation

9.1 Frequency Modulation

The minimum and maximum frequencies of the frequency modulation output can be configured via GUI on the Configure\DOUT tab. The frequency accuracy of the Frequency Modulation Output is determined by the frequency accuracy of the internal oscillator. Compensation mathematics for temperature drift of the oscillator is described in subsection 6.6.

Table 65: FOUT Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
FOUT _{MIN}	Minimum output frequency		100		255	Hz
FOUT _{MAX}	Maximum output frequency		1000		10000	Hz
FOUT _{ERR}	Frequency error	FOUT feature operated with non-compensated internal oscillator clock	-5%		5%	

9.2 Pulse Width Modulation

PWM can be enabled and configured via GUI on the Configure\DOUT tab. PWM base frequency can be adjusted according to Table 66.

Table 66: PWM Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
PWM _{BaseFreq}	PWM Base Frequency	Stepsize: 500Hz in range 0.5kHz to 15kHz	0.2	0.5	15	kHz

10 Digital Interfaces

10.1 Serial Interfaces

For sensor data read out, ZSSC3281 supports three digital interface protocols in slave mode operation:

- I2C/I3C
- SPI
- OWI (One-Wire-Interface)

Digital slave interfaces do not initiate data communication with the master system themselves but have to quickly react on arbitrary received read/write requests from the master.

To maintain short response times in continuous Cyclic Mode operation, ZSSC3281 is equipped with a dedicated DMA controller, which can read the content of the SSC Process Image (see subsection 6.3) without interaction of the ARM MCU.

The DMA controller supports one active digital interface at the time. After reset, the DMA controller activates and locks the serial interface for further communication that first received a valid telegram. A telegram is valid if:

- the address match was pass for I2C/I3C or OWI and the first 8-bit of telegram data were received
- the Slave Select (SS) was activated for SPI and first 8-bit of telegram data were received on MOSI

As soon as one of the three interfaces was locked by DMA controller, potential data streams from the other interfaces are blocked. A different interface can only be selected after reset of ZSSC3281.

10.1.1 Command / Response Format

All three interfaces operate on the same command request and response format. The number of data bytes which need to follow the command byte in the command request or are returned after the Status Byte in command response, assuming the command execution was completed, is specific to the command code.

Table 67: Command Request Format

Command	Command Byte								Data Bytes
	7	6	5	4	3	2	1	0	
Valid Command	8-bit command								[Data Bytes]

Table 68: I2C Command Response Format

Command	Command Byte								Data Bytes
	7	6	5	4	3	2	1	0	
Previously received command in execution, response pending, New command not accepted, retry later	Telegram Error Flag	Power Supply OK	Busy Flag	1	SSC Mode 00: Command Mode 01: Cyclic Mode 10: Sleep Mode 11: Boot/Diagnosis Mode	Memory Error	Sensor Connection Fault	Saturation ¹	NONE
Command successfully processed				0					[Data Bytes]

¹ Cleared before each command execution except for 0x80 and 0x81 Read Output Memory commands, 0xA8 Start Sleep Mode command, and 0xA9 Start Command Mode.

A list of supported command codes, the number of command and response data bytes and the command function description can be found in subsection 10.5.

If a command is still processed by the ZSSC3281 when the response read starts, the BusyFlag of the Status Byte is set and no response data is returned. The response data stream only contains a repeated Status Byte until the transaction is ended. The BusyFlag within the Status Byte changes as soon as the command execution is completed.

10.1.2 Advanced Error Response

Beside the command and response format there is an option for an advanced error response. This option can be enabled in the GUI at the tab Configure\System Control and supports failure detection during communication with ZSSC3281.

If this feature is enabled, it will replace the Status Byte with an Error Response Byte in case that a command error as shown in Table 69 was detected. This Error Response Byte will be repeated continuously as long as the host requests data. By this replacement it can easily be detected if a command error was detected since the MSB of the error response byte is set. MSB is cleared in case of a normal Status Byte.

Table 69: Command Response Format

Command Status	Error Response Byte (MSB always set)	
	Error Code	Interpretation of Error Code
Command unknown in Cyclic Mode	0x80	Not Successful
Command failed or not known Command		
Command CRC Byte aborted/missing (if protocol CRC was enabled)	0x90	Incomplete Command CRC failed
Expected Data CRC Byte aborted/missing (only possible if protocol CRC was enabled)		Incomplete
Mandatory data aborted		
Command CRC failed (only possible if protocol CRC was enabled)	0x82	CRC Error
Data CRC failed (only possible if protocol CRC was enabled)		
Command not authorized	0xA0	Not Authorized
Mandatory data not in range	0xB0	Argument Error

10.2 I2C/I3C

ZSSC3281 supports I2C communication in StandardMode, FastMode, FastMode+, and it supports high speed communication in I3C Single Data Rate (SDR) Mode on I2C SCL and I2C SDA pins. The I2C/I3C interface is listening to receive a telegram after system startup or system reset as long as the SPI Slave Select (pin SPI SS) signal is not active.

I2C/I3C communication mode is selected and locked after I2C/I3C address match was pass and the first 8-bit of telegram data were received.

The interface settings, and a selection whether to use the traditional I2C or the advanced I3C communication mode, can be made in the GUI at the tab Configure\Serial Interfaces in section I2C/I3C.

I3C is an MIPI standard <https://www.mipi.org/specifications/i3c-sensor-specification> which is based on the traditional I2C protocol but extends the physical layer and the protocol layer towards higher communication speeds and improved management of the slave communication parameters by the I3C master. It allows In-Band Interrupts through which an I3C slave can signal an interrupt request to the I3C master via the SCL/SDA lines. Inband Interrupts are not supported by ZSSC3281.

Table 70: I2C/I3C Interface Parameter

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
SlvAddr	I2C slave address	ZSSC3281 delivery default		0x3C		
	Static I3C address					
f _{SCL}	Interface clock	I2C Mode	0.1		1.0	MHz
		I3C Mode	0.1		12.5	MHz
D _{I2C}	Duty cycle		33	–	50	%

Timing and protocol details of the I2C communication in Standard Mode, Fast Mode, and Fast Mode+ are given in I2C-Bus Specification, Rev.6, UM10204. SCL Clock Stretching is not supported by ZSSC3281.

In I2C/I3C Mode, each Command Request follows the structure shown in Figure 57. Only the number of Data Bytes needed by the command must be sent.

Command Request (I2C/I3C Write)

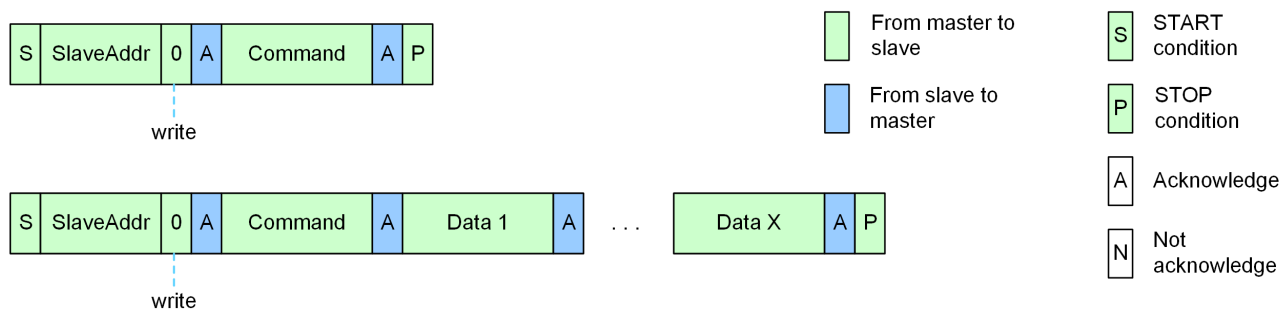


Figure 57: I2C/I3C Command Request

The different options for a response request are shown in Figure 58.

Read Data (I2C/I3C Read)

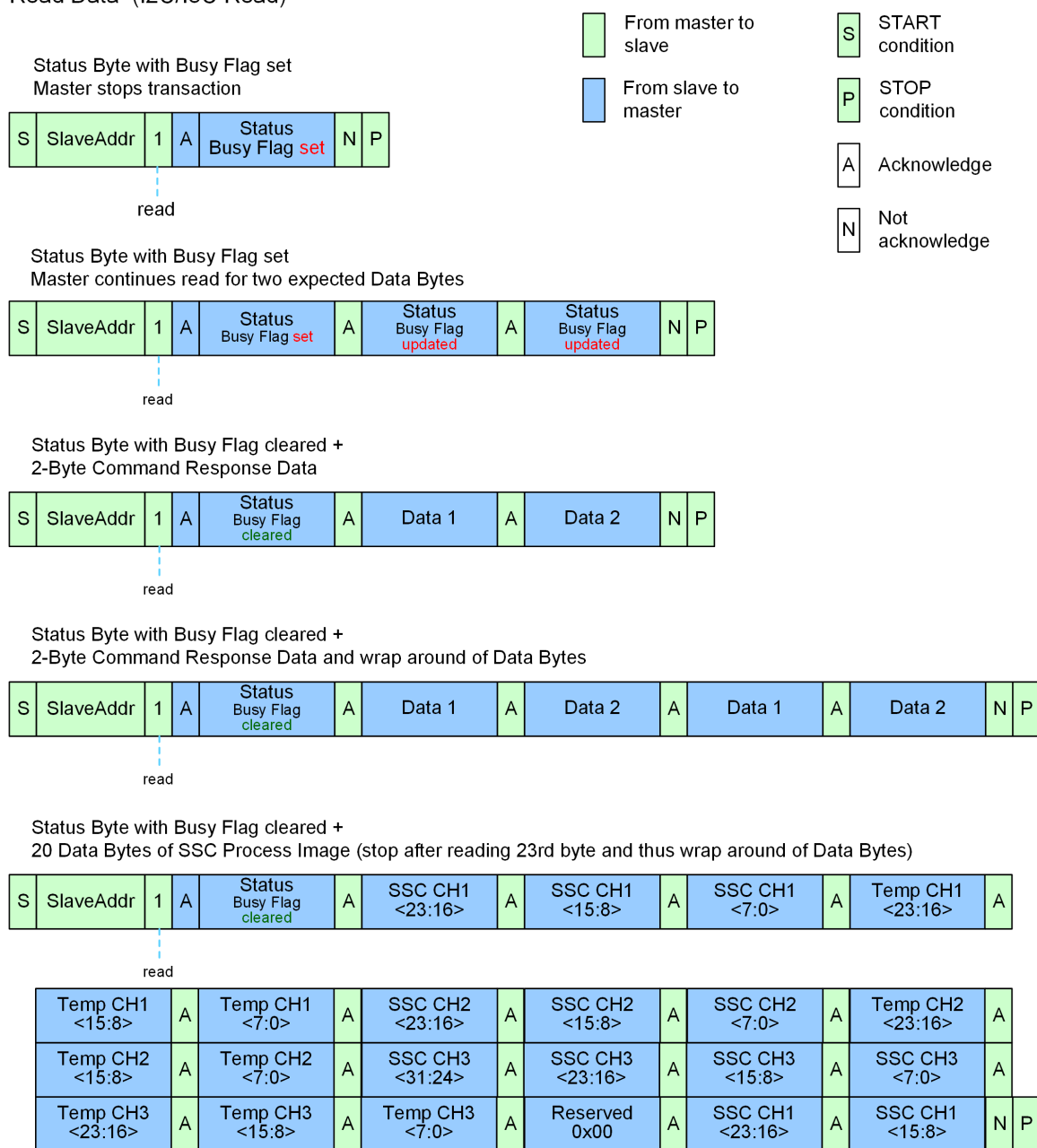


Figure 58: I2C/I3C Response Request

10.2.1 CRC

The I2C communication can be protected using CRC bytes see Equation 57. To enable this feature, both this option and the advanced error response (see subsubsection 10.1.2) must be activated. The first CRC byte is transmitted after the address and command byte (in requests) or after the address and command response byte (in responses). Subsequently, a CRC byte is transmitted after every second byte, as illustrated in Figure 59. Both the communication master and slave must be configured for CRC protection mode before communication begins. A CRC-protected communication is valid only if:

- At least one CRC check is performed
- All evaluated CRCs are correct
- The last transmitted byte is a CRC byte

$$CRC8, x^8 + x^2 + x + 1 \text{ seed } 0xA5 \quad (57)$$

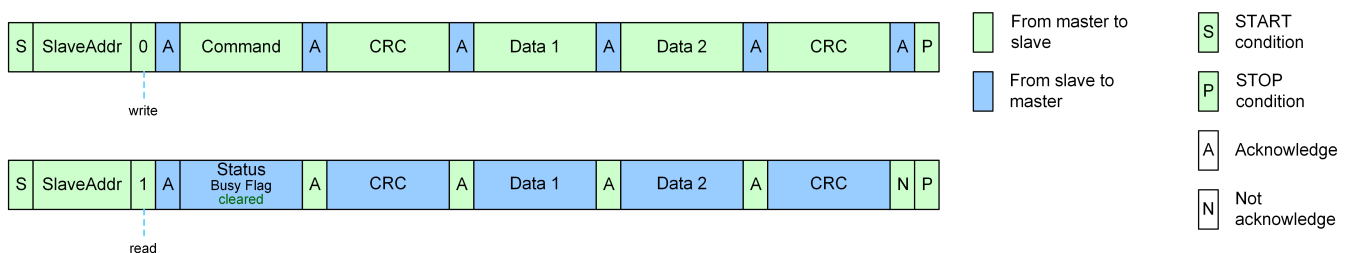


Figure 59: I2C/I3C Communication Including CRC Protection

10.2.2 I2C Address Pin Selection

The ZSSC3281 provides the option to define the two LSBs of the I2C address via two GPIOs: I2C Address PinSel 0 (GPIO5) and I2C Address PinSel 1 (GPIO6). When enabled, this feature overrides the predefined I2C address stored in *I3cslvRegStatAddrCtrl.Addr* register. The GPIO-defined address bits are combined with the CCP-defined address bits immediately after power-on, ensuring the ZSSC3281 has only one valid I2C address. This pin selection option must be activated via *I3cslvRegStatAddrCtrl.PinSel*. When enabled, internal pull-up resistors are activated on I2C Address PinSel 0 (GPIO5) and I2C Address PinSel 1 (GPIO6), ensuring well-defined operation even when pins are left unconnected. The pin logic operates as follows:

- Floating pin (unconnected): respective bit is forced to logical '0'
- Pin shorted to VSS: respective bit is forced to logical '1'

This logic is shown in Table 71.

Table 71: I2C Slave Address Register

	I2C Address						
I2C Address Bit Location	6	5	4	3	2	1	0
GPIO Configurable	only via CCP configuration					GPIO6	GPIO5
Default Value (0x3C)	0	1	1	1	1	'high / floating' = 0 'low' = 1	'high / floating' = 0 'low' = 1
	Defined by <i>I3cslvRegStatAddrCtrl.Addr</i>						

10.3 SPI

ZSSC3281 supports SPI communication on the SPI SCLK, SPI MOSI, and SPI MISO pins if the SPI slave select signal is active at the SPI SS pin and no other serial interface was locked yet after reset or power-on.

An active SPI SS signal connects the SPI SCLK and SPI MOSI pins to the SPI slave interface at the DMA controller and disconnects the I2C/I3C slave. As soon as the first 8-bit of data received on MOSI line, the SPI interface is locked as communication interface until the next reset or power-on of the ZSSC3281.

The polarity of the SPI slave select signal is active low by delivery default. It can be changed to active high at the Serial Interfaces tab of the GUI Configure\Serial Interfaces\SPI Slave Select Polarity. The polarity and the phase of the SPI clock can be changed via 'CPHA' and 'CPOL' selection fields at the same GUI tab.

The different combinations of polarity and phase are illustrated in Figure 60 and Figure 61. See Table Table 72 for the timing parameters.

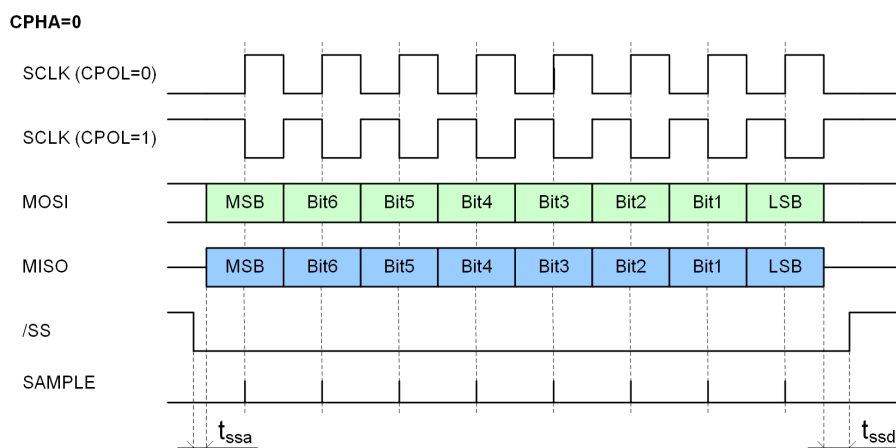


Figure 60: SPI Configuration CPHA=0

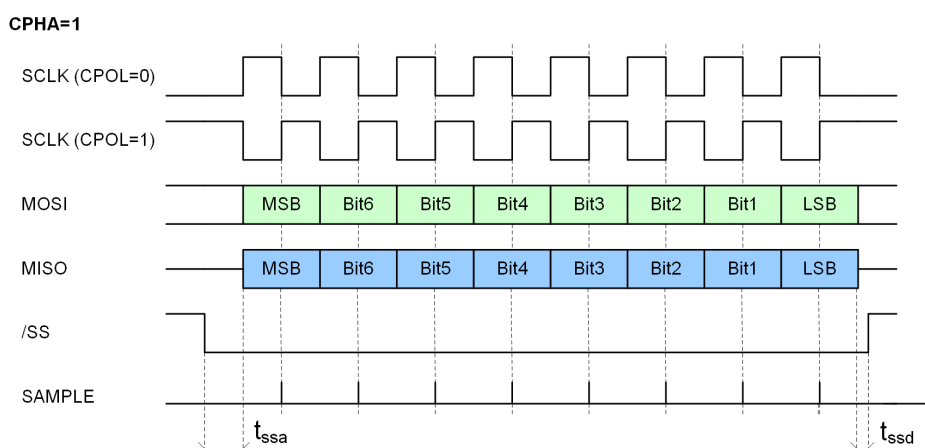


Figure 61: SPI Configuration CPHA=1

Table 72: SPI Interface Parameter

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{SCLK}	Interface clock		0.05	1	12	MHz
D_{SPI}	Duty cycle		40	50	60	%
SR_{SPI}	Input rising and falling edge slew rate		0.26		1	V/ns
t_{ssa}	Delay time between SS-activation edge and first edge of SLCK, MOSI or MISO	"Typical" is for $f_{SCLK} \leq 3\text{MHz}$ operation	62.5			ns
t_{ssd}	Delay time between SS-deactivation edge and last edge of SLCK, MOSI or MISO			50		ns
t_{ss}	Delay between SS-deactivation edge of last command and of SS-activation edge for next command		10			μs

In SPI Mode, each command request follows the structure shown in Figure 63. Only the number of data bytes needed by the command must be sent.

A SPI transaction is started with activation of SPI SS and it is ended with deactivation of SPI SS. A new command request can only be sent at the start of a new transaction, which begins after SPI SS changed from inactive to active state.

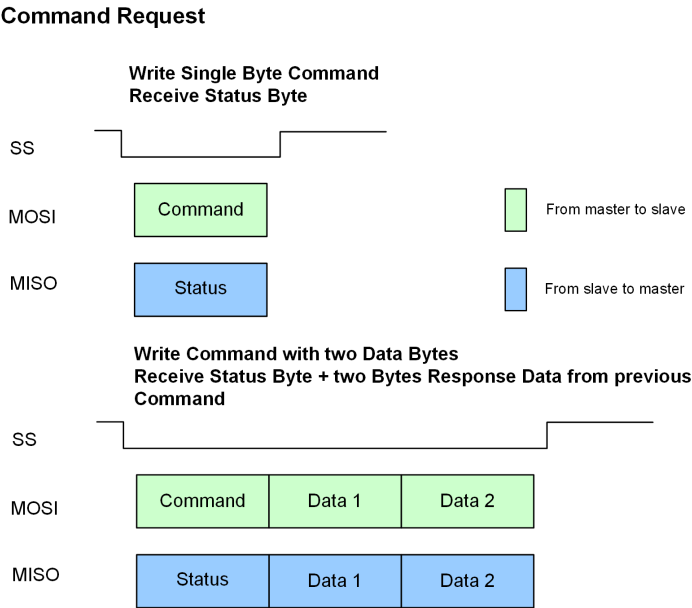


Figure 62: SPI Command Request

In contrast to the I2C/I3C interface the SPI interface supports full duplex communication. Hence, a new command request can already be sent on the MOSI line while response data from the previous command request is returned on the MISO line. According to Figure 62 and Figure 63 ZSSC3281 always responds with Status Byte, even at the very first reading.

If the response data from the previous call is read without triggering a new command request in parallel, the NOP command must be sent on the MOSI line in the first telegram byte of the transaction as shown in Figure 63.

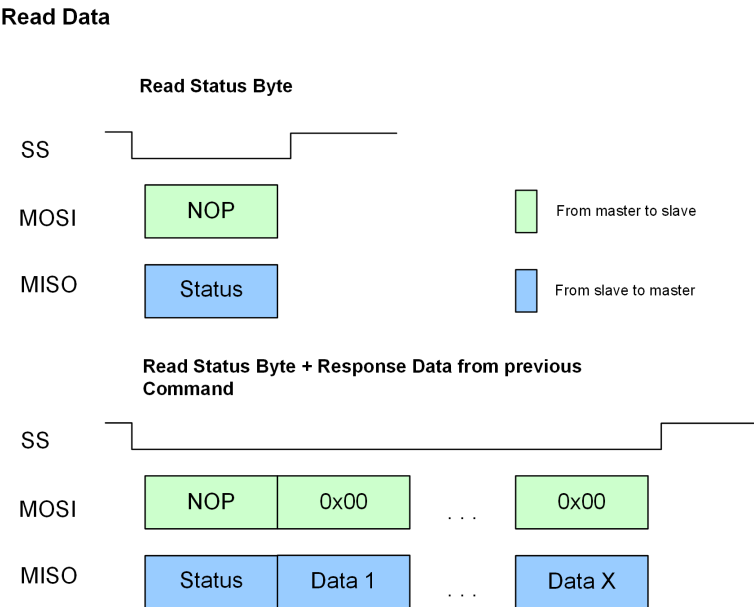


Figure 63: SPI Read Data

10.4 One-Wire-Interface

ZSSC3281 employs a one-wire digital interface (OWI) concept. The communication principle of the OWI interface is derived from the I2C protocol.

An advantage of the OWI is that it enables “end of line” calibration, no additional pins are required to digitally calibrate a finished assembly sensor module. Although the OWI is integrated mainly for calibration, it can also be used to read out the calibrated sensor signal continuously or retrieve diagnostic detail information.

The OWI driver and the OWI receiver are usually connected both to the analog output signal pin AOUT. The mode switching at AOUT between Analog Output Mode and OWI Communication Mode is controlled via different selectable OWI operation modes that are described in subsection 10.4.1.

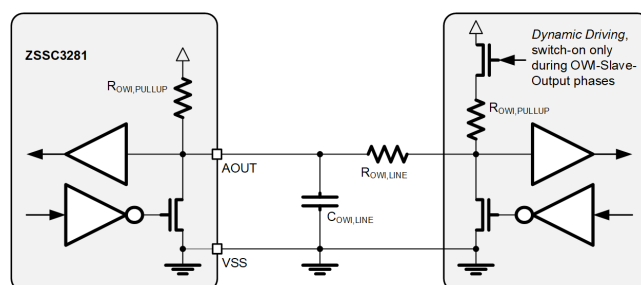


Figure 64: General Block Schematic of the OWI Interface

Some Analog Output configurations, like 2-Wire and 3-Wire Current Loop Mode and the 10V Absolute Voltage Mode require a second OWI input pin (OWI-IN2) because the external AOUT circuitry does not allow to drive a digital signal from an external OWI master into the AOUT pin. A respective application schematic is provided in subsection 13.3 and subsection 13.4.

The OWI protocol is defined as follows:

Idle state	During inactivity of the bus, the OWI line is pulled up to the supply voltage VDD by an external resistor.
Start condition	When the OWI line is in idle mode, a low pulse with a minimum width of $t_{OWI,START} \geq 10\mu s$ and then a return to high indicates a start condition. Every request must be initiated by a start condition sent by a master. A master can generate a start condition only when the OWI line is in idle mode.
Stop condition	A constant level at the OWI line (no transition from low to high or from high to low) for at least twice the period of the last transmitted valid bit indicates a stop condition. Without considering the last bit-time, a stop condition is generated with a constant level at the OWI line for at least 20ms. The master finishes a transmission by changing back to the high level (idle mode). Every command must be closed by a stop condition to start the processing of the command. The master must interrupt a sending slave after it has completed a data request by clamping the OWI line to the low level for generating a stop condition.
Valid data	Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB). Transmitted bits are recognized after a start condition at every transition from low to high at the OWI line. The value of the transmitted bit depends on the duty ratio between the high phase and high/low period (bit period, $t_{OWI,BIT}$ in Table 74). A duty ratio greater than 1/8 and less than 3/8 is detected as 0; a duty ratio greater than 5/8 and less than 7/8 is detected as 1. The bit period of consecutive bits must not increase to more than 1.5 times the previous bit period or decrease to less than half of the previous bit period because a stop condition is detected in this case.
Write operation	During transmission from master to slave (WRITE), the address byte including a set data direction bit (0 for WRITE) is followed by a command byte and, depending on the transmitted command, by an optional number of data bytes. The internal ARM MCU evaluates the received command and processes the requested routine. Figure 65 illustrates the writing of a command with two data bytes and a command without data bytes.

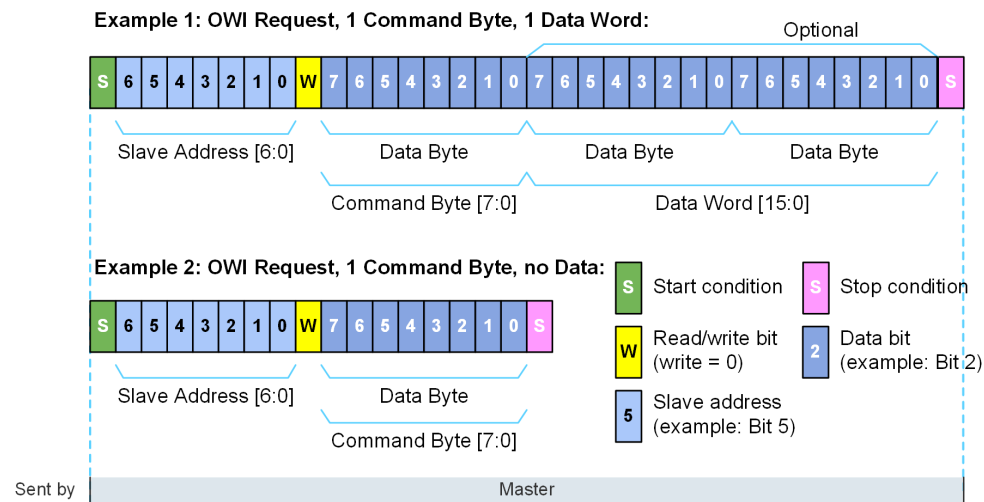


Figure 65: OWI Write Operation/Command Request

Read operation

After a data read request from the master to the slave (matching address byte and data direction bit = 1 for READ), the slave answers by sending data from the interface output registers. The master must generate a stop condition after receiving the requested data (see Figure 66). The data in the output registers is sent continuously until a stop condition is detected. After transmitting all available data, the slave starts repeating the data. The data of an ongoing OWI transaction is fixed. It does not get updated with newly available conditioned results. To receive new output data a new OWI read transaction must be started.

Example: OWI Read Operation, Status Byte (+n) Data Bytes*:

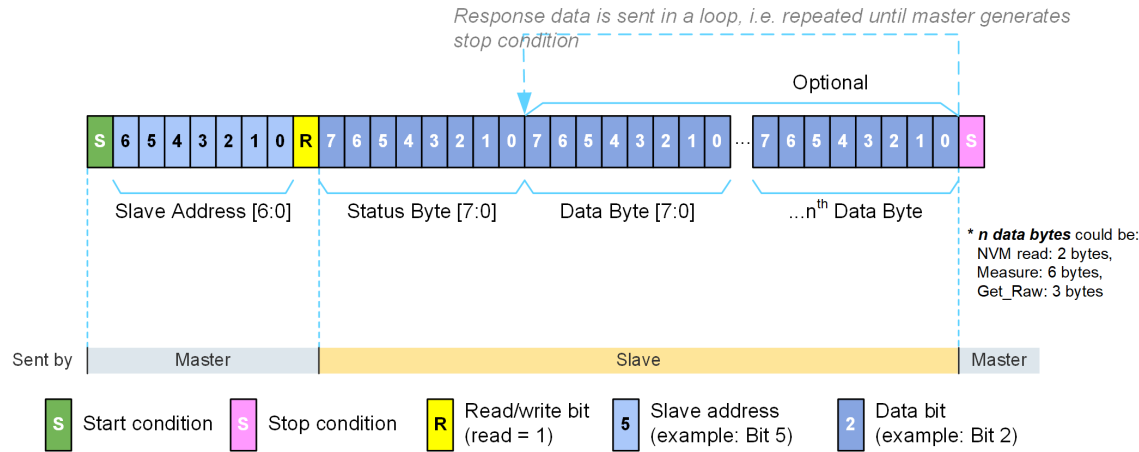


Figure 66: OWI Read Operation

The length of the OWI-line and the size of ROWI,PULL (if it is statically connected to AOUT), and consequently the resistive and capacitive loads, influence the maximum possible interface speed and minimum bit period. Additional capacitance on the OWI1 (AOUT) line can improve RF disturbance robustness und harsh EMC conditions. Table 73 shows practical OWI interface dimensioning examples and the resulting maximum signal frequencies (minimum possible bit periods).

The ZSSC3281's OWI interface properties and timing capabilities are given in Table 74.

Table 73: OWI Dimensioning Examples

		$R_{OWI,PULL} (+ R_{OWI,LOAD})$				
		1.8 k Ω	2.5 k Ω	3.3 k Ω	5.5 k Ω	10.0 k Ω
C _{OWI,LOAD}	1nF	20 μ s	20 μ s	21 μ s	35 μ s	63 μ s
	10nF	113 μ s	157 μ s	207 μ s	345 μ s	628 μ s
	22nF	249 μ s	345 μ s	456 μ s	760 μ s	1381 μ s
	33nF	373 μ s	518 μ s	684 μ s	1140 μ s	2070 μ s
	44nF	497 μ s	691 μ s	912 μ s	1520 μ s	2762 μ s
	51nF	576 μ s	801 μ s	1057 μ s	1760 μ s	3205 μ s

¹ Examples are shown with statically connected $R_{OWI,PULL}$, and with minimum bit period: $t_{OWI,BIT}$.

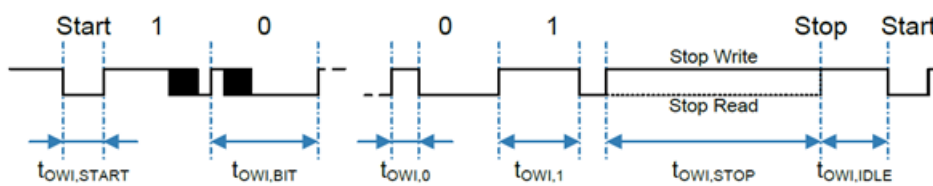


Figure 67: OWI Telegram

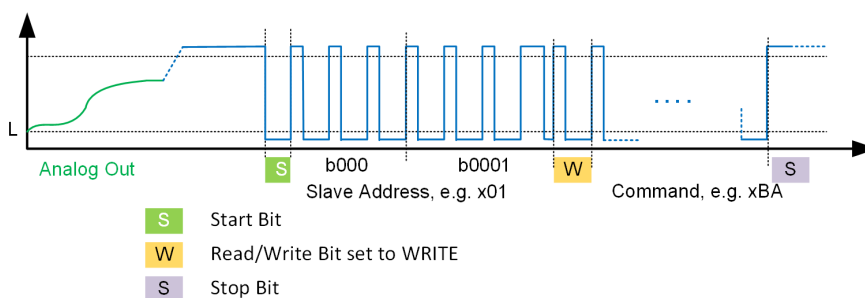


Figure 68: Typical OWI Communication on AOUT in Voltage Out Mode

Table 74: OWI Timing Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$t_{OWI,WINDOW}$	OWI-Startup "Listening" Window	Time after power-on in which the OWI can be enabled by a valid OWI-Start-Condition and command				ms
		OWI Window Mode		400		
		OWI Analog Mode		200		
$t_{OWI,IDLE}$	Bus free time between start and stop condition		1	30		μ s
$t_{OWI,START}$	Hold time start condition		10			μ s
$t_{OWI,BIT}$	Bit time		10	40	4000	μ s
$t_{OWI,0}$	Duty ratio bit '0'		0.125	0.25	0.375	$t_{OWI,BIT}$
$t_{OWI,1}$	Duty ratio bit '1'		0.625	0.75	0.875	$t_{OWI,BIT}$
t_{OWI,BIT_DEV}	Bit time deviation	Tolerated variation of Bit time from bit to bit	0.55	1.0	1.45	$t_{OWI,BIT}$
$t_{OWI,STOP}$	Hold time stop condition	t_{OWI,BIT_L} is the bit time of the last valid bit	1.5	2.5		t_{OWI,BIT_L}
C _{OWI,LOAD}	Capacitive load at OWI line		–	2.2	50	nF
$R_{OWI,PULL}$	Pull-up resistance – master		0.3	0.47	3.3	k Ω
$R_{OWI,LOAD}$	Resistive OWI line load		20	0.01 x $R_{OWI,PULL}$	–	Ω

An enabled OWI interface is checked after power-on or reset of ZSSC3281 for incoming telegrams. The OWI interface is locked by DMA controller for further communication if it is the first which received a telegram with a matching slave address and at least 8bit of telegram data. The OWI communication mode can only be left by power-on or reset of the ZSSC3281.

10.4.1 OWI operation modes

The ZSSC3281 allows utilization of the OWI interface in different application configurations. The respective configuration settings can be made in the GUI via Configure\Serial Interfaces\OWI Mode.

OWI Disable/OWI Off	This mode deactivates the OWI interface. For example, this could be applied in cases when an analog-output smart sensor is configured and calibrated using the OWI interface and the OWI is not available for end user access after calibration and final setup/programming.
OWI Digital (no analog output)	In this mode AOUT does not provide any analog outputs and is only used as OWI pin. There is no startup window limitation for activation of the OWI interface, but if the ZSSC3281 was started in Command Mode or Sleep Mode and no OWI Startup (0xBA) command was received within a window time of 200ms, the system state machine automatically moves to Cyclic Mode.
OWI Window	<p>The OWI Window Mode is not intended to be used in end applications but useful to run with calibration line due to easier access to OWI communication. The OWI Window Mode disables the analog output signal driving at AOUT after power-on or reset of ZSSC3281 for a startup window time of $2 \times 200\text{ms}$. During the first 200ms window ZSSC3281 listens on OWI-IN1 (=AOUT) for incoming OWI telegrams. As soon as it receives an OWI Startup (0xBA) command on OWI-IN1 it locks the AOUT channel for OWI communication. The OWI channel can only be locked if the I2C/I3C and SPI channels remained silent and do not lock the interface first.</p> <p>If no OWI Startup command was received during the first 200ms startup window, a second 200ms window is started and ZSSC3281 listens on OWI-IN2 for incoming OWI telegrams. If it detects an OWI Startup (0xBA) command within the second 200ms startup window, it locks the OWI channel to the OWI-IN2 + AOUT communication path.</p> <p>If no OWI Startup command was received even during the second 200ms startup window, the OWI interface is disabled automatically and the AOUT resumes to its configured analog output function. OWI Window Mode is the factory default OWI mode for AOUT.</p>
OWI Analog Voltage	<p>The OWI Analog Voltage mode allows to start OWI communication even while the configured voltage output function is already active on AOUT. During a startup window of 200ms after power-on or reset ZSSC3281 listens on OWI-IN1 for incoming OWI telegrams. As soon as it receives an OWI Startup (0xBA) command on OWI-IN1 it locks the AOUT channel for OWI communication.</p> <p>The difference to the OWI Window Mode is, that the OWI master has to overdrive the analog output voltage signal at AOUT. To prevent self-locking of the OWI channel without external overdrive from the OWI master (for example, if the conditioned analog output waveform at AOUT matches an OWI telegram by accident), the OWI slave also checks for the occurrence of at least one overdrive drive condition at AOUT (either short to VSS or short to VDD) before it releases a received OWI telegram to the DMA Controller.</p> <p>If no OWI Startup command was received during the 200ms startup window, the OWI interface is disabled automatically and the AOUT remains in its configured analog output function. OWI activation is not possible until new power-on or reset of ZSSC3281.</p>

10.5 Command Interpreter

The availability of commands in Table 75 depends on the active main operating mode (Command or Cyclic Mode) and the current connection mode.

Some commands require an additional argument for successful command execution. If an argument error or missing argument appears, the current command is not executed and a failure is indicated in the extended error response.

Table 75: Command List

Command Code (Byte)	Return (after Status Byte)	Description	Command Available in		
			Sleep Mode	Command Mode	Cyclic Mode
0x80	20-byte SCC data	Read output memory Reads content of output memory which contains following information: <ul style="list-style-type: none"> • Conditioned Bridge Sensor1 (24-bit) • Conditioned Temperature Channel1 (24-bit) • Conditioned Sensor2 (24-bit) • Conditioned Temperature Channel2 (24-bit) • Logic Bridge Sensor Channel3 (32-bit) • Conditioned Temperature Channel3 (24-bit) • Reserved byte (0x00) (8-bit) Note: <ul style="list-style-type: none"> • If more than 20 data bytes are read by the host, the response data rolls over. • In Command Mode or Sleep Mode the last valid output data is provided. 	Yes	Yes ³	Yes
0x81 followed by data 0xXXYY	0xYY bytes	Read output memory burst Reads content of output memory in burst mode: <ul style="list-style-type: none"> • 0xXX selects the byte in output memory which is read first • 0xYY defines the number of bytes which is read from output memory Note: If more than 0xYY data bytes are read by the host, the response data rolls over. In Command Mode or Sleep Mode the last valid output data is provided.	Yes	Yes ³	Yes
0x82 followed by 0xXX + 0xWW	0xWW × 4 bytes	Read configuration data in burst Reads content of Configuration and Calibration Page (CCP) in burst mode: <ul style="list-style-type: none"> • 0xXX selects the 32-bit word in CCP which is read first • 0xWW defines the number of words which is read from output memory Note: Maximum supported 0xWW is 0x20		Yes ³	
0x83 followed by data 0xXXWW	—	(Over-) Write configuration data in burst ¹ Writes content of Configuration and Calibration Page (CCP) in burst mode into Shadow RAM: <ul style="list-style-type: none"> • 0xXX selects the word in CCP which is written first • 0xWW defines the number of words which is written in output memory Note: Maximum supported 0xWW is 0x20		Yes ³	
0x84 followed by 0xXX + 0xWW	0xWW × 4 bytes	Read device info data in burst Reads device info data in burst mode : <ul style="list-style-type: none"> • 0xXX selects the word in InfoPage which is read first • 0xWW defines the number of words which is read from output memory Note: Maximum supported 0xXX is 0x1F Note: Maximum supported 0xWW is 0x20 Note: If 0xXX + 0xWW is > 0x20, the command fails.		Yes ³	
0x88	—	Copy CCP RAM shadow to flash Programs Configuration and Calibration Page in flash with content from Shadow RAM		Yes ³	
0x89	4 bytes (CCP version with PID)	Read expected CCP Version		Yes ³	
0x8A	2 bytes	Read chip revision Returns 0x0003		Yes ³	
0x8B	3 bytes (Bootloader Version)	Read IAP Version Returns 0x010000		Yes ³	
0x8C	No answer is returned (Execution jumps directly to the FW update routines)	Start firmware update Triggers Firmware update procedure.		Yes ³	
0x8D	n.a. (Device is immediately restarted)	Restart the Device		Yes ³	

Continued on next page

Table 75: Command List (Continued)

Command Code (Byte)	Return (after Status Byte)	Description	Command Available in		
			Sleep Mode	Command Mode	Cyclic Mode
0x8E	3 bytes (APP Firmware Version)	Read RCA Firmware Version Returns 0x010600002db849c5		Yes ³	
0xA0	1 bytes raw data (Previously executed command code)	Read Last Executed Command returns command code of last executed command	Yes	Yes ³	
0xA1 followed by 0xXX + 0xYY	3 bytes (Raw data)	Extended Raw Sensor Measurement ² Returns unconditioned and raw sensor data from different points of the data path 0xXX: AFE to measure from • 0: AFE1 • 1: AFE2 0xYY: Measurement point in the data path to measure • 0: Raw (same as other raw measurement commands) • 1: Raw _{Scaled} (before 1/C linearization) • 2: Raw _{Adc} (before any capacitive pre-calculation) Note: If the channel is unavailable, a zero value is returned (e.g. cap. Mode 5 with measurement points 0 or 1 for AFE2).	Yes	Yes ³	
0xA2	3 bytes raw data	Raw sensor measurement AFE1 ² Returns unconditioned raw data of Bridge Sensor1	Yes	Yes ³	
0xA3	3 bytes raw data	Raw sensor measurement AFE2 ² Returns unconditioned raw data of Bridge Sensor2 If AFE2 is disabled, an error response is returned. Note: If the channel is unavailable, a zero value is returned (e.g. Capacitive Application Mode 5).	Yes	Yes ³	
0xA4	3 bytes raw data	Raw temperature measurement Sensor1 ² Returns unconditioned temperature data for Temperature Channel 1	Yes	Yes ³	
0xA5	3 bytes raw data	Raw temperature measurement Sensor2 ² Returns unconditioned temperature data for Temperature Channel 2	Yes	Yes ³	
0xA6	3 bytes raw data	Raw temperature measurement Sensor3 ² Returns unconditioned temperature data for Temperature Channel 3	Yes	Yes ³	
0xA7 followed by 0xXX + 0xYY	20 bytes (Raw data)	Snapshot calibration all sensors ² Returns unconditioned raw sensor and temperature data of all AFE channels that are activated in CCP. Other auxiliary measurement tasks will be excluded within the execution of this command. • 0xXX minimum average count for AFE1 data • 0xYY minimum average count for AFE2 data 0xXX and 0xYY must be in range 1 to 32 (=0x20). "Minimum average count" defines the minimal amount of executed measurement task within one measurement cycle. Typically, those are single temperature or auto-zero measurement tasks. Thus, main measurements like SM+ and SM- might be executed more often. The output data format is as follows: • Raw Data Bridge Sensor1 (24 bit) • Raw Data Temperature Channel1 (24 bit) • Raw Data Bridge Sensor2 (24 bit) • Raw Data Temperature Channel2 (24 bit) • 0x00000000 (4 bytes 0x0) (32 bit) • Raw Data Temperature Channel3 (24 bit) • 0x00 (1 byte 0x0) (8 bit)	Yes	Yes ³	
0xA8	–	START_SLEEP Exit Command Mode or Cyclic Mode and transition to Sleep Mode	Yes	Yes ³	Yes
0xA9	–	Start Command Mode Exit Cyclic Mode and transition to Command Mode Note To verify the completion of a command, the user must check the entire status byte, including both the busy bit and the SSC mode.	Yes	Yes ³	Yes

Continued on next page

Table 75: Command List (Continued)

Command Code (Byte)	Return (after Status Byte)	Description	Command Available in		
			Sleep Mode	Command Mode	Cyclic Mode
0xAA followed by data 0xXXYY	20 bytes SSC data (Fully corrected sensor measurement data plus corrected temperature data)	Snapshot measurement all sensors ² Returns conditioned sensor and temperature data of all AFE channels that are activated in CCP. <ul style="list-style-type: none"> • 0xXX minimum average count for AFE1 data • 0xYY minimum average count for AFE2 data 0xXX and 0xYY must be in range 1 to 32 (=0x20). The output data format is as follows: <ul style="list-style-type: none"> • Bridge Sensor1 (24-bit) • Temperature Channel1 (24-bit) • Bridge Sensor2 (24-bit) • Temperature Channel2 (24-bit) • Third Logic Channel Combination (4 bytes 0x0) (32-bit) • Temperature Channel3 (24-bit) • Reserved byte (0x00) (8-bit) 	Yes	Yes ³	
0xAB	-	Start Cyclic Mode Enter Cyclic Mode based on configuration in Shadow RAM: continuous measurement cycles, SSC corrections, and automatic, continuous digital and/or analog output updates	Yes	Yes ³	
0xB0	12 bytes diagnostic result data	Read diagnosis status Responds with the detailed diagnosis status (see subsection 7.2)	Yes	Yes ³	
0xB1	—	Reset diagnosis status Resets the contents of the diagnosis status register to 0x00	Yes	Yes ³	
0xB2 followed by data (0x0000 to 0xFFFF)	-	Update diagnosis status Executes all activated sensor and system diagnosis checks Note: If a measurement cycle is running concurrently, the diagnostic update happens after completion of the measurement cycle and SSC calculations.	Yes ³	Yes ³	
0xB3 followed by data (0x0000 to 0xFFFF)	-	Direct DAC Stimulus Set the DAC output register with the data in the command and enable/output the respective analog signal through AOUT (according to the AOUT_setup) Note: The DAC output can be switched off by the RESN pin, POR, or a change in the main operating mode		Yes ³	
0xB4 followed by 0x0X + 0xYY	2 bytes	Self-diagnostic measure for AFE1 and AFE2 Parameter 0x0X: <ul style="list-style-type: none"> • AFE1: 0x00 • AFE2: 0x01 • Parameter 0xYY See description in Table 58		Yes ³	
0xB5 followed by 0xXX 0xYY 0xYY 0xYY	n.a.	Direct linear stimulus of analog output path Stimulates the output path, linear relation between input data and pin output. Parameter 0xXX - Output Selection: <ul style="list-style-type: none"> • 0: reserved • 1: AOUT • 2: reserved • 3: reserved Parameter 0xYYYYYY – Output Value: <ul style="list-style-type: none"> • 24bit data value for output, unsigned integer (as SSC value format) • assigned output is static (the output can be switched off by the RESN pin, POR, or a change in the main operating mode) Note: The following workflow for the given command must be ensured: <ul style="list-style-type: none"> • Start Command Mode (0xA9) • Set Direct linear stimulus of output path (0xB5) • Reset the device 		Yes ³	
0xB8	12 bytes (diagnostic result data)	Read fault memory Responds with the detailed fault-memory status (see subsection 7.2)		Yes ³	

Continued on next page

Table 75: Command List (Continued)

Command Code (Byte)	Return (after Status Byte)	Description	Command Available in		
			Sleep Mode	Command Mode	Cyclic Mode
0xB9	n.a.	Reset fault memory Resets the contents of the fault memory to 0x0		Yes ³	
0xBA	–	Startup OWI Initialization command to enter OWI interface operation; only valid for OWI (see subsection 10.4.1)		Yes ³	Yes
0xFF	Status followed by last output buffer data	NOP Output of read results; only valid for SPI	Yes	Yes ³	Yes

¹ The Overwrite CCP data command 0x83 can be used to optimize evaluation and test routine execution time for analog front-end setup or to configure measurement setups without changing the ZSSC3281's Flash content. Without adding command 0x88 the changes made by 0x83 command are lost after reset of ZSSC3281 reset via the RESN pin or Power On Reset.

² These commands can be used to conduct a measurement with or without SSC conditioning, e.g., during the smart sensor calibration procedure. No digital correction is performed on the measurement result except for the Snapshot measurement all sensors (0xAA) command. The setup and configuration for the raw measurement is the content in the shadow registers that can be pre-loaded (automatically loaded during power-on) from the Flash or by means of the Overwrite command 0x83.

Use Oversample measurements to obtain noise-minimized measurement results in Sleep or Command Mode. With higher oversampling factors, the command execution time increases proportionally.

³ Command is also available after entering Command Mode from Static Diagnostic Mode (SDM).

11 Firmware Update

ZSSC3281 offers a firmware update function via the serial I2C interface for Renesas provided code (RCA code).

Figure 69 shows the high-level firmware flow. Initiating the firmware update is done by a “start firmware update” command in command mode. This command stores a command sequence in a dedicated register and performs a reset of the device. Due to the required command sequence, the device starts to the update procedure during system boot and performs the firmware update.

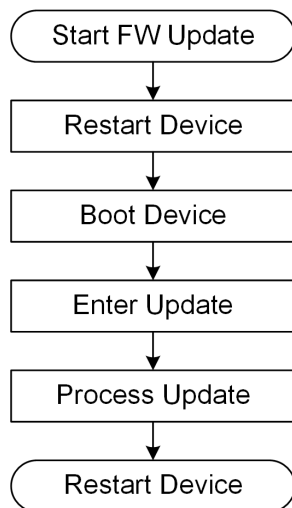


Figure 69: High-level Firmware Update Flow

A firmware update is meant to be executed exclusively via the ZSSC3281 GUI. It can be initiated at the FW Update Tab, where the respective new firmware file can be selected, and the update process can be triggered.

12 Configuration and Calibration Page (CCP) Memory Map

This section describes the details and usage of single bitfields of CCP memory. The bitfields have two possible access attributes:

- **Reserved:** contains data that is set by Renesas and must not be changed from its default value.
- **Read/Write:** programmable with proper Read/Write access. By default all bitfields can be assumed as read and writeable. Thus an empty access information indicates an read and writeable bitfield.

12.1 Serial Interfaces

12.1.1 0x00 – IfbParamCfg

Address : 0x00		Register Name : IfbParamCfg		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:5	Reserved	0x0		Reserved
4		0x0	BypassCmdInterp	Bypass of IFB Command Interpreter in Cyclic Mode 0x0 : Inactive 0x1 : Active
3	Reserved	0x0		Reserved
2		0x0	EnErrResp	Extended Error Response Mode in Serial Communication 0x0 : Inactive 0x1 : Active
1		0x0	EnCrc	CRC Checking of Serial Interface Communication 0x0 : Disabled 0x1 : Enabled

12.1.2 0x01 – I3cslvRegCtrl

Address : 0x01		Register Name : I3cslvRegCtrl		Default: 0x000000C0
Bits	Access	Default	Field Name	Description
31:8	Reserved	0x0		Reserved
7		0x1	Model2c	Operation Mode of I2C/I3C Interface 0x0 : I3C Mode 0x1 : I2C Mode
6		0x1	Enable	I2C/I3C Interface Activation 0x0 : Disabled 0x1 : Enabled
5:4	Reserved	0x0		Reserved
3:0		0x0	Instanceld	I3C Instance ID 4bit hex value

12.1.3 0x02 – I3cslvRegStatAddrCtrl

Address : 0x02		Register Name : I3cslvRegStatAddrCtrl		Default: 0x0000003C
Bits	Access	Default	Field Name	Description
31:17	Reserved	0x0		Reserved
16		0x0	PinSel	I2C Address Selection via Pins
15:7	Reserved	0x0		Reserved
6:0		0x3C	Addr	I2C/I3C Static Slave Address 7bit hex value

12.1.4 0x03 – I3cslvInBandIrqSupport

Address : 0x03		Register Name : I3cslvInBandIrqSupport		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:1	Reserved	0x0		Reserved
0		0x0	InBandIrq	I2C/I3C Inband Interrupt Support 0x0 : Disabled 0x1 : Enabled

12.1.5 0x04 – SpislvParamCfg

Address : 0x04		Register Name : SpislvParamCfg		Default: 0x00000001
Bits	Access	Default	Field Name	Description
31:4	Reserved	0x0		Reserved
3		0x0	SsPolar	SPI Slave Select Polarity 0x0 : Active Low 0x1 : Active High
2		0x0	ClockPolar	SPI Clock Polarity 0x0 : CPOL =0; Default Low 0x1 : CPOL=1; Default High
1		0x0	ClockPhase	ISPI Clock Phase 0x0 : CPHA=0 0x1 : CPHA=1
0		0x1	Enable	SPI Interface Activation 0x0 : Disabled 0x1 : Enabled

12.1.6 0x05 – OwislvCtrReg

Address : 0x05		Register Name : OwislvCtrReg		Default: 0x00000008
Bits	Access	Default	Field Name	Description
31:8	Reserved	0x0		Reserved
7		0x0	OutPolarBit	OWI-OUT Output Polarity 0x0 : Active Low 0x1 : Active High
6		0x0	In2PolarBit	OWI-IN2 Input Polarity 0x0 : Active Low 0x1 : Active High
5		0x0	In1PolarBit	OWI-IN1 Input Polarity 0x0 : Active Low 0x1 : Active High
4	Reserved	0x0		Reserved
3		0x1	SlvAddrEn	OWI Slave Address Checking 0x0 : Disabled 0x1 : Enabled
2		0x0	FammAddrEn	Family address enable
1		0x0	FixedLenEn	Apply fixed bit length as defined in register OwislvFixedlenReg for transmission instead of the bit length measured for the last received bit. 0x0 : Disabled 0x1 : Enabled

12.1.7 0x06 – OwislvSlvaddrReg

Address : 0x06		Register Name : OwislvSlvaddrReg		Default: 0x00000028
Bits	Access	Default	Field Name	Description
31:7	Reserved	0x0		Reserved
6:0		0x28	SlvAddr	OWI Static Slave Address 7bit hex value

12.1.8 0x07 – OwislVFixedlenReg

Address : 0x07		Register Name : OwislVFixedlenReg		Default: 0x00000140
Bits	Access	Default	Field Name	Description
31:16	Reserved	0x0		Reserved
15:0		0x140	FixedLen	Bit length of a single OWI bit in 8MHz clock cycles, relevant only if OwislVCtrReg.FixedLenEn = 1 16bit hex value

12.1.9 0x08 – OwiModeParam

Address : 0x08		Register Name : OwiModeParam		Default: 0x00000001
Bits	Access	Default	Field Name	Description
31:3	Reserved	0x0		Reserved
2:0		0x1	OwislVMode	OWI Slave Operation Mode 0x0 : Off 0x1 : Window 0x2 : Digital 0x3 : Analog5V 0x4 : Analog10V 0x5 : AnalogCL2 0x6 : AnalogCL3 Note: Window as operation mode is not intended to be used in end application.

12.1.10 0x09 – CntCommParam

Address : 0x09		Register Name : CntCommParam		Default: 0x0000000A
Bits	Access	Default	Field Name	Description
31:0		0xA	CntCommParam	Internal parameter of ZSSC3281 Firmware. Must not be changed.

12.1.11 0x0A – CommParamCrc

Address : 0x0A		Register Name : CommParamCrc		Default: 0x685AD4EB
Bits	Access	Default	Field Name	Description
31:0		0x685AD4EB	CommParamCrc	Internal parameter of ZSSC3281 Firmware. Must not be changed.

12.2 Clocks

12.2.1 0x0B – MiscctrlParamCfg.Clkout

Address : 0x0B		Register Name : MiscctrlParamCfg.Clkout		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:2	Reserved	0x0		Reserved
1:0		0x0	Clkoutmode	Clock Output Signal at CLK_OUT Pin (GPIO14) 0x0 : Inactive 0x1 : Internal High Speed Clock (16MHz) 0x2 : Internal Low Speed Clock (32kHz) 0x3 : Main System Clock depends on setting in Register MiscctrlParamCfg.Divfclk

12.2.2 0x0C – MiscctrlParamCfg.Divafeaout

Address : 0x0C		Register Name : MiscctrlParamCfg.Divafeaout		Default: 0x00000008
Bits	Access	Default	Field Name	Description
31:6	Reserved	0x0		Reserved
5		0x0	Afe2LowSpeedMode	AFE2 clock speed with respect to AFE1 0x0 : Normal (equal) Speed 0x1 : Quarter Speed
4:2		0x2	FreqDivClkAout	Clock Divider HighSpeedClock to AFE Clock 0x0 : div1 (16MHz AOUT clock) 0x1 : div2 (8MHz AOUT clock) 0x2 : div4 (4MHz AOUT clock) 0x3 : div8 (2MHz AOUT clock) 0x4 : div16 (1MHz AOUT clock)
1:0		0x0	FreqDivClkAfe	Clock Divider HighSpeedClock to AFE Clock 0x0 : div4 (4MHz AFE clock) 0x1 : div8 (2MHz AFE clock) 0x2 : div16 (1MHz AFE clock)

12.2.3 0x0D – MiscctrlParamCfg.Divfclk

Address : 0x0D		Register Name : MiscctrlParamCfg.Divfclk		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:3	Reserved	0x0		Reserved
2:0		0x0	Divfclk	Clock Divider HighSpeedClock to AFE Clock 0x0 : div1 (16MHz AOUT clock) 0x1 : div2 (8MHz AOUT clock) 0x2 : div4 (4MHz AOUT clock) 0x3 : div8 (2MHz AOUT clock) 0x4 : div16 (1MHz AOUT clock)

12.2.4 0x0E – SmuParamCfg.Anacfg

Address : 0x0E		Register Name : SmuParamCfg.Anacfg		Default: 0x00000108
Bits	Access	Default	Field Name	Description
31:9	Reserved	0x0		Reserved
8:4		0x10	ExtldoVolt	External JFET LDO Voltage if SmuParamCfg.Anacfg.ExtldoDisable set to enabled 0x02 : 3.00V 0x04 : 4.00V 0x08 : 5.00V 0x10 : 5.25V
3		0x1	PgLossDetect	Power-Ground Loss Activation 0x0 : Enabled 0x1 : Disabled
2:1	Reserved	0x0		Reserved
0		0x0	ExtldoDisable	External JFET LDO Activation 0x0 : Enabled 0x1 : Disabled

12.2.5 0x0F – SmuParamCfg.Extclkcfg

Address : 0x0F		Register Name : SmuParamCfg.Extclkcfg		Default: 0x00271030
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:8		0x2710	WaitTime	
7	Reserved	0x0		Reserved
6:4		0x3	StartupTime	
3	Reserved	0x0		Reserved
2		0x0	Type	External Clock Type 0x0 : Clock
1		0x0	EnExtclk	External Clock Input Activation 0x0 : Disabled

12.2.6 0x10 – AfeBaseCfgParam

Address : 0x10		Register Name : AfeBaseCfgParam		Default: 0x00000003
Bits	Access	Default	Field Name	Description
31:24		0x0	AfeSyncStatus	AFE1 / AFE2 Synchronization 0x0 : Asynchronous measurement 0x1 : Synchronized measurement
23:16		0x0	Afe2SmConfig	AFE2 Sequencer Configuration 0x0 : SM- and SM+ 0x1 : SM+ and AUX_AZ 0x2 : SM+ only 0x3 : No Main Sensor-Bridge Measurement 0x4 : Capacitive SM+ and SM-
15:8		0x0	Afe1SmConfig	AFE1 Sequencer Configuration 0x0 : SM- and SM+ 0x1 : SM+ and AUX_AZ 0x2 : SM+ only 0x3 : No Main Sensor-Bridge Measurement 0x4 : Capacitive SM+ and SM-
7:0		0x3	AfeActive	AFE Activation configuration 0x0 : None 0x1 : AFE1 only 0x2 : AFE2 only 0x3 : AFE1 and AFE2 0x7 : DualSpeed

12.2.7 0x11 – AfeBaseCfgParam.AfeDsCfg.Reg1

Address : 0x11		Register Name : AfeBaseCfgParam.AfeDsCfg.Reg1		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24		0x0	ConvCnt	Internal Dual Speed Mode parameter - Must not be changed.
23:0		0x0	Thresh1	Dual Speed Mode Threshold 1

12.2.8 0x12 – AfeBaseCfgParam.AfeDsCfg.Reg2

Address : 0x12		Register Name : AfeBaseCfgParam.AfeDsCfg.Reg2		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	Thresh2	Dual Speed Mode Threshold 2

12.3 Basic AFE Setup

12.3.1 0x13 – Bm1Cfg1

Address : 0x13		Register Name : Bm1Cfg1		Default: 0x04000655
Bits	Access	Default	Field Name	Description
31		0x0	BmType	Sensor Type 0x0 : Resistive Bridge 0x1 : Thermopile / Thermocouple
30	Reserved	0x0	BmTestDac	Reserved, must remain 0
29	Reserved	0x0	BmTest	Reserved, must remain 0
28:26		0x1	BmAdcMux	ADC Input MUX Setting 0x0 : ADC inputs shorted to AGND 0x1 : ADC input connected to PGA 0x2 : ADC input connected to input (Gain = 1, PGA bypassed)
25:22		0x0	BmBrdgRtl	Rtl resistor, applicable if BmBrdgType = 1 0x0 : Open 0x4 : 8000Ω 0x8 : 20000Ω 0x1 : 1333Ω 0x5 : 10000Ω 0x9 : 24000Ω 0x2 : 2000Ω 0x6 : 14000Ω 0xA : 28000Ω 0x3 : 4000Ω 0x7 : 18000Ω 0xB : 40000Ω
21:18		0x0	BmBrdgRth	Rth resistor, applicable if BmBrdgType = 1 0x0 : Open 0x4 : 8000Ω 0x8 : 20000Ω 0x1 : 1333Ω 0x5 : 10000Ω 0x9 : 24000Ω 0x2 : 2000Ω 0x6 : 14000Ω 0xA : 28000Ω 0x3 : 4000Ω 0x7 : 18000Ω 0xB : 40000Ω
17:16		0x0	BmSetTime	Bridge Settling Time before ADC conversion starts 0x0 : 20μs 0x1 : 40μs 0x2 : 60μs 0x3 : 80μs
15		0x0	BmBrdgType	Bridge Supply via TOPx, BOTx 0x0 : Voltage Source 0x1 : Resistor or Current Source
14:12		0x0	BmAdcShift	ADC Shift V_{Shift} / V_{fs} 0x0 : 0 0x2 : 0.250 0x4 : 0.500 0x6 : 0.750 0x1 : 0.125 0x3 : 0.375 0x5 : 0.625 0x7 : 0.875
11:8		0x6	BmAdcReso	ADC Resolution 0x0 : 10 Bit 0x4 : 14 Bit 0x8 : 18 Bit 0xC : 22 Bit 0x1 : 11 Bit 0x5 : 15 Bit 0x9 : 19 Bit 0xD : 23 Bit 0x2 : 12 Bit 0x6 : 16 Bit 0xA : 20 Bit 0xE : 24 Bit 0x3 : 13 Bit 0x7 : 17 Bit 0xB : 21 Bit
7		0x0	BmPgaPolarity	PGA Polarity 0x0 : Positive 0x1 : Negative
6:4		0x5	BmPgaGain2	PGA2 Gain 0x0 : 1.1 0x2 : 1.3 0x4 : 1.5 0x6 : 1.7 0x1 : 1.2 0x3 : 1.4 0x5 : 1.6 0x7 : 1.8
3:0		0x5	BmPgaGain1	PGA1 Gain 0x0 : 1.2 0x3 : 5.97 0x6 : 29.6 0x9 : 76.6 0xC : 187 0x1 : 2 0x4 : 11.9 0x7 : 39.2 0xA : 112 0xD : 223 0x2 : 4 0x5 : 19.8 0x8 : 58.1 0xB : 143 0xE : 275

12.3.2 0x14 – Bm1Cfg2

Address : 0x14		Register Name : Bm1Cfg2		Default: 0x00000210	
Bits	Access	Default	Field Name	Description	
31:15	Reserved	0x0		Reserved	
14		0x0	BmSetPerm	Enables permanent bridge supply	
13:12		0x0	BmSetTimeMult	Bridge settling time multiplier	
11:10		0x0	BmBias	AFE Bias Current Setting 0x0 : normal operation 0x3 : reduced AFE bias current	
9		0x1	BmAdcEnShift	ADC Shift & Gain ×2 Enable, activates BmAdcShift setting 0x0 : ADC Gain ×1, ADC Shift disabled 0x3 : ADC Gain ×2, ADC Shift enabled	
8:5		0x0	BmBrdglBias	Sensor Supply Current, applicable if BmBrdgType = 1 0x0 : Open/Off 0x4 : 40μA 0x8 : 200μA 0x1 : 5μA 0x5 : 80μA 0x9 : 500μA 0x2 : 10μA 0x6 : 100μA 0x3 : 20μA 0x7 : 160μA	
4:0		0x10	BmPgaOffset	PGA Offset Shift 0x1 : -1.9mV 0x10 : 0mV 0x2 : -3.8mV 0x11 : 1.9mV 0x3 : -5.6mV 0x12 : 3.8mV 0x4 : -7.5mV 0x13 : 5.6mV 0x5 : -9.4mV 0x14 : 7.5mV 0x6 : -11.3mV 0x15 : 9.4mV 0x7 : -13.1mV 0x16 : 11.3mV 0x8 : -15.0mV 0x17 : 13.1mV 0x9 : -16.9mV 0x18 : 15.0mV 0xA : -18.8mV 0x19 : 16.9mV 0xB : -20.6mV 0x1A : 18.8mV 0xC : -22.5mV 0x1B : 20.6mV 0xD : -24.4mV 0x1C : 22.5mV 0xE : -26.2mV 0x1D : 24.4mV 0xF : -28.1mV 0x1E : 26.2mV 0x1F : 28.1mV	

12.3.3 0x15 – Bm2Cfg1

Address : 0x15		Register Name : Bm2Cfg1		Default: 0x04000656
Bits	Access	Default	Field Name	Description
31		0x0	BmType	Sensor Type 0x0 : Resistive Bridge 0x1 : Thermopile / Thermocouple
30	Reserved	0x0	BmTestDac	Reserved, must remain 0
29	Reserved	0x0	BmTest	Reserved, must remain 0
28:26		0x1	BmAdcMux	ADC Input MUX Setting 0x0 : ADC inputs shorted to AGND 0x1 : ADC input connected to PGA 0x2 : ADC input connected to input (Gain = 1, PGA bypassed)
25:22		0x0	BmBrdgRtl	Rtl resistor, applicable if BmBrdgType = 1 0x0 : Open 0x4 : 8000Ω 0x8 : 20000Ω 0x1 : 1333Ω 0x5 : 10000Ω 0x9 : 24000Ω 0x2 : 2000Ω 0x6 : 14000Ω 0xA : 28000Ω 0x3 : 4000Ω 0x7 : 18000Ω 0xB : 40000Ω
21:18		0x0	BmBrdgRth	Rth resistor, applicable if BmBrdgType = 1 0x0 : Open 0x4 : 8000Ω 0x8 : 20000Ω 0x1 : 1333Ω 0x5 : 10000Ω 0x9 : 24000Ω 0x2 : 2000Ω 0x6 : 14000Ω 0xA : 28000Ω 0x3 : 4000Ω 0x7 : 18000Ω 0xB : 40000Ω
17:16		0x0	BmSetTime	Bridge Settling Time before ADC conversion starts 0x0 : 20μs 0x1 : 40μs 0x2 : 60μs 0x3 : 80μs
15		0x0	BmBrdgType	Bridge Supply via TOPx, BOTx 0x0 : Voltage Source 0x1 : Resistor or Current Source
14:12		0x0	BmAdcShift	ADC Shift $V_{\text{Shift}} / V_{\text{fs}}$ 0x0 : 0 0x2 : 0.250 0x4 : 0.500 0x6 : 0.750 0x1 : 0.125 0x3 : 0.375 0x5 : 0.625 0x7 : 0.875
11:8		0x6	BmAdcReso	ADC Resolution 0x0 : 10 Bit 0x4 : 14 Bit 0x8 : 18 Bit 0xC : 22 Bit 0x1 : 11 Bit 0x5 : 15 Bit 0x9 : 19 Bit 0xD : 23 Bit 0x2 : 12 Bit 0x6 : 16 Bit 0xA : 20 Bit 0xE : 24 Bit 0x3 : 13 Bit 0x7 : 17 Bit 0xB : 21 Bit
7		0x0	BmPgaPolarity	PGA Polarity 0x0 : Positive 0x1 : Negative
6:4		0x5	BmPgaGain2	PGA2 Gain 0x0 : 1.1 0x2 : 1.3 0x4 : 1.5 0x6 : 1.7 0x1 : 1.2 0x3 : 1.4 0x5 : 1.6 0x7 : 1.8
3:0		0x6	BmPgaGain1	PGA1 Gain 0x0 : 1.2 0x3 : 5.97 0x6 : 29.6 0x9 : 76.6 0xC : 187 0x1 : 2 0x4 : 11.9 0x7 : 39.2 0xA : 112 0xD : 223 0x2 : 4 0x5 : 19.8 0x8 : 58.1 0xB : 143 0xE : 275

12.3.4 0x16 – Bm2Cfg2

Address : 0x16		Register Name : Bm2Cfg2		Default: 0x00000210	
Bits	Access	Default	Field Name	Description	
31:15	Reserved	0x0		Reserved	
14		0x0	BmSetPerm	Enables permanent bridge supply	
13:12		0x0	BmSetTimeMult	Bridge settling time multiplier	
11:10		0x0	BmBias	AFE Bias Current Setting 0x0 : normal operation 0x3 : reduced AFE bias current	
9		0x1	BmAdcEnShift	ADC Shift & Gain ×2 Enable, activates BmAdcShift setting 0x0 : ADC Gain ×1, ADC Shift disabled 0x3 : ADC Gain ×2, ADC Shift enabled	
8:5		0x0	BmBrdglBias	Sensor Supply Current, applicable if BmBrdgType = 1 0x0 : Open/Off 0x4 : 40μA 0x8 : 200μA 0x1 : 5μA 0x5 : 80μA 0x9 : 500μA 0x2 : 10μA 0x6 : 100μA 0x3 : 20μA 0x7 : 160μA	
4:0		0x10	BmPgaOffset	PGA Offset Shift 0x1 : -1.9mV 0x10 : 0mV 0x2 : -3.8mV 0x11 : 1.9mV 0x3 : -5.6mV 0x12 : 3.8mV 0x4 : -7.5mV 0x13 : 5.6mV 0x5 : -9.4mV 0x14 : 7.5mV 0x6 : -11.3mV 0x15 : 9.4mV 0x7 : -13.1mV 0x16 : 11.3mV 0x8 : -15.0mV 0x17 : 13.1mV 0x9 : -16.9mV 0x18 : 15.0mV 0xA : -18.8mV 0x19 : 16.9mV 0xB : -20.6mV 0x1A : 18.8mV 0xC : -22.5mV 0x1B : 20.6mV 0xD : -24.4mV 0x1C : 22.5mV 0xE : -26.2mV 0x1D : 24.4mV 0xF : -28.1mV 0x1E : 26.2mV 0x1F : 28.1mV	

12.4 External Temperature Sensor

12.4.1 0x17 – ExtTemp1Cfg1

Address : 0x17		Register Name : ExtTemp1Cfg1		Default: 0x0011C5F1					
Bits	Access	Default	Field Name	Description					
31:28	Reserved	0x0		Reserved					
27:24		0x0	ExtTempBrdgRtl	Rtl resistor, applicable if BmBrdgType = 1 0x0 : Open 0x4 : 8000Ω 0x8 : 20000Ω 0x1 : 1333Ω 0x5 : 10000Ω 0x9 : 24000Ω 0x2 : 2000Ω 0x6 : 14000Ω 0xA : 28000Ω 0x3 : 4000Ω 0x7 : 18000Ω 0xB : 40000Ω					
23:20		0x1	ExtTempBrdgRth	Rth resistor, applicable if BmBrdgType = 1 0x0 : Open 0x4 : 8000Ω 0x8 : 20000Ω 0x1 : 1333Ω 0x5 : 10000Ω 0x9 : 24000Ω 0x2 : 2000Ω 0x6 : 14000Ω 0xA : 28000Ω 0x3 : 4000Ω 0x7 : 18000Ω 0xB : 40000Ω					
19		0x0	ExtTempInput	External Temperature Sensor Input MUX 0x0 : Input connected to PGA 0x1 : Input connected to ADC					
18:15		0x3	ExtTempType	External Temperature Type 0x0 : Reserved 0x1 : Diode/NTC/PTC sink mode, internal bias 0x2 : Diode/NTC/PTC, external bias 0x3 : Diode/NTC/PTC source mode, internal bias 0x4 : Reserved 0x5 : Bridge single ended, internal bias 0x6 : Bridge single ended, external bias 0x7 : Bridge differential					
14:12		0x4	ExtTempAdcShift	ADC Shift $V_{\text{Shift}} / V_{\text{fs}}$ 0x0 : 0 0x2 : 0.250 0x4 : 0.500 0x6 : 0.750 0x1 : 0.125 0x3 : 0.375 0x5 : 0.625 0x7 : 0.875					
11:8		0x5	ExtTempAdcReso	ADC Resolution 0x0 : 10 Bit 0x2 : 12 Bit 0x4 : 14 Bit 0x1 : 11 Bit 0x3 : 13 Bit 0x5 : 15 Bit					
7		0x1	ExtTempPgaPolarity	PGA Polarity 0x0 : Positive 0x1 : Negative					
6:4		0x7	ExtTempPgaGain2	PGA2 Gain 0x0 : 1.1 0x2 : 1.3 0x4 : 1.5 0x6 : 1.7 0x1 : 1.2 0x3 : 1.4 0x5 : 1.6 0x7 : 1.8					
3:0		0x1	ExtTempPgaGain1	PGA1 Gain 0x0 : 1.2 0x3 : 5.97 0x6 : 29.6 0x9 : 76.6 0xC : 187 0x1 : 2 0x4 : 11.9 0x7 : 39.2 0xA : 112 0xD : 223 0x2 : 4 0x5 : 19.8 0x8 : 58.1 0xB : 143 0xE : 275					

12.4.2 0x18 – ExtTemp1Cfg2

Address : 0x18		Register Name : ExtTemp1Cfg2		Default: 0x00000210	
Bits	Access	Default	Field Name	Description	
31:14	Reserved	0x0		Reserved	
13:12		0x0	ExtTempSetTime	T1 Input Settling Time before ADC conversion starts 0x0 : 20μs 0x1 : 40μs 0x2 : 60μs 0x3 : 80μs	
11:10		0x0	ExtTempBias	AFE Bias Current Setting 0x0 : normal operation 0x3 : reduced AFE bias current	
9		0x1	ExtTempAdcEnShift	ADC Shift & Gain ×2 Enable, activates BmAdcShift setting 0x0 : ADC Gain ×1, ADC Shift disabled 0x3 : ADC Gain ×2, ADC Shift enabled	
8:5		0x0	ExtTempBrdglBias	Sensor Supply Current, applicable if BmBrdgType = 1 0x0 : Open/Off 0x4 : 40μA 0x8 : 200μA 0x1 : 5μA 0x5 : 80μA 0x9 : 500μA 0x2 : 10μA 0x6 : 100μA 0x3 : 20μA 0x7 : 160μA	
4:0		0x10	ExtTempPgaOffset	PGA Offset Shift 0x1 : -1.9mV 0x10 : 0mV 0x2 : -3.8mV 0x11 : 1.9mV 0x3 : -5.6mV 0x12 : 3.8mV 0x4 : -7.5mV 0x13 : 5.6mV 0x5 : -9.4mV 0x14 : 7.5mV 0x6 : -11.3mV 0x15 : 9.4mV 0x7 : -13.1mV 0x16 : 11.3mV 0x8 : -15.0mV 0x17 : 13.1mV 0x9 : -16.9mV 0x18 : 15.0mV 0xA : -18.8mV 0x19 : 16.9mV 0xB : -20.6mV 0x1A : 18.8mV 0xC : -22.5mV 0x1B : 20.6mV 0xD : -24.4mV 0x1C : 22.5mV 0xE : -26.2mV 0x1D : 24.4mV 0xF : -28.1mV 0x1E : 26.2mV 0x1F : 28.1mV	

12.4.3 0x19 – ExtTemp2Cfg1

Address : 0x19		Register Name : ExtTemp2Cfg1		Default: 0x00118502				
Bits	Access	Default	Field Name	Description				
31:28	Reserved	0x0		Reserved				
27:24		0x0	ExtTempBrdgRtl	Rtl resistor, applicable if BmBrdgType = 1 0x0 : Open 0x4 : 8000Ω 0x8 : 20000Ω 0x1 : 1333Ω 0x5 : 10000Ω 0x9 : 24000Ω 0x2 : 2000Ω 0x6 : 14000Ω 0xA : 28000Ω 0x3 : 4000Ω 0x7 : 18000Ω 0xB : 40000Ω				
23:20		0x1	ExtTempBrdgRth	Rth resistor, applicable if BmBrdgType = 1 0x0 : Open 0x4 : 8000Ω 0x8 : 20000Ω 0x1 : 1333Ω 0x5 : 10000Ω 0x9 : 24000Ω 0x2 : 2000Ω 0x6 : 14000Ω 0xA : 28000Ω 0x3 : 4000Ω 0x7 : 18000Ω 0xB : 40000Ω				
19		0x0	ExtTempInput	External Temperature Sensor Input MUX 0x0 : Input connected to PGA 0x1 : Input connected to ADC				
18:15		0x3	ExtTempType	External Temperature Type 0x0 : Reserved 0x1 : Diode/NTC/PTC sink mode, internal bias 0x2 : Diode/NTC/PTC, external bias 0x3 : Diode/NTC/PTC source mode, internal bias 0x4 : Reserved 0x5 : Bridge single ended, internal bias 0x6 : Bridge single ended, external bias 0x7 : Bridge differential				
14:12		0x0	ExtTempAdcShift	ADC Shift V_{Shift} / V_{fs} 0x0 : 0 0x2 : 0.250 0x4 : 0.500 0x6 : 0.750 0x1 : 0.125 0x3 : 0.375 0x5 : 0.625 0x7 : 0.875				
11:8		0x5	ExtTempAdcReso	ADC Resolution 0x0 : 10 Bit 0x2 : 12 Bit 0x4 : 14 Bit 0x1 : 11 Bit 0x3 : 13 Bit 0x5 : 15 Bit				
7		0x0	ExtTempPgaPolarity	PGA Polarity 0x0 : Positive 0x1 : Negative				
6:4		0x0	ExtTempPgaGain2	PGA2 Gain 0x0 : 1.1 0x2 : 1.3 0x4 : 1.5 0x6 : 1.7 0x1 : 1.2 0x3 : 1.4 0x5 : 1.6 0x7 : 1.8				
3:0		0x2	ExtTempPgaGain1	PGA1 Gain 0x0 : 1.2 0x3 : 5.97 0x6 : 29.6 0x9 : 76.6 0xC : 187 0x1 : 2 0x4 : 11.9 0x7 : 39.2 0xA : 112 0xD : 223 0x2 : 4 0x5 : 19.8 0x8 : 58.1 0xB : 143 0xE : 275				

12.4.4 0x1A – ExtTemp2Cfg2

Address : 0x1A		Register Name : ExtTemp2Cfg2		Default: 0x00000010	
Bits	Access	Default	Field Name	Description	
31:14	Reserved	0x0		Reserved	
13:12		0x0	ExtTempSetTime	T1 Input Settling Time before ADC conversion starts 0x0 : 20μs 0x1 : 40μs 0x2 : 60μs 0x3 : 80μs	
11:10		0x0	ExtTempBias	AFE Bias Current Setting 0x0 : normal operation 0x3 : reduced AFE bias current	
9		0x0	ExtTempAdcEnShift	ADC Shift & Gain ×2 Enable, activates BmAdcShift setting 0x0 : ADC Gain ×1, ADC Shift disabled 0x3 : ADC Gain ×2, ADC Shift enabled	
8:5		0x0	ExtTempBrdglBias	Sensor Supply Current, applicable if BmBrdgType = 1 0x0 : Open/Off 0x4 : 40μA 0x8 : 200μA 0x1 : 5μA 0x5 : 80μA 0x9 : 500μA 0x2 : 10μA 0x6 : 100μA 0x3 : 20μA 0x7 : 160μA	
4:0		0x10	ExtTempPgaOffset	PGA Offset Shift 0x1 : -1.9mV 0x10 : 0mV 0x2 : -3.8mV 0x11 : 1.9mV 0x3 : -5.6mV 0x12 : 3.8mV 0x4 : -7.5mV 0x13 : 5.6mV 0x5 : -9.4mV 0x14 : 7.5mV 0x6 : -11.3mV 0x15 : 9.4mV 0x7 : -13.1mV 0x16 : 11.3mV 0x8 : -15.0mV 0x17 : 13.1mV 0x9 : -16.9mV 0x18 : 15.0mV 0xA : -18.8mV 0x19 : 16.9mV 0xB : -20.6mV 0x1A : 18.8mV 0xC : -22.5mV 0x1B : 20.6mV 0xD : -24.4mV 0x1C : 22.5mV 0xE : -26.2mV 0x1D : 24.4mV 0xF : -28.1mV 0x1E : 26.2mV 0x1F : 28.1mV	

12.4.5 0x1B – ExtTemp3Cfg1

Address : 0x1B		Register Name : ExtTemp3Cfg1		Default: 0x00118502				
Bits	Access	Default	Field Name	Description				
31:28	Reserved	0x0		Reserved				
27:24		0x0	ExtTempBrdgRtl	Rtl resistor, applicable if BmBrdgType = 1 0x0 : Open 0x4 : 8000Ω 0x8 : 20000Ω 0x1 : 1333Ω 0x5 : 10000Ω 0x9 : 24000Ω 0x2 : 2000Ω 0x6 : 14000Ω 0xA : 28000Ω 0x3 : 4000Ω 0x7 : 18000Ω 0xB : 40000Ω				
23:20		0x1	ExtTempBrdgRth	Rth resistor, applicable if BmBrdgType = 1 0x0 : Open 0x4 : 8000Ω 0x8 : 20000Ω 0x1 : 1333Ω 0x5 : 10000Ω 0x9 : 24000Ω 0x2 : 2000Ω 0x6 : 14000Ω 0xA : 28000Ω 0x3 : 4000Ω 0x7 : 18000Ω 0xB : 40000Ω				
19		0x0	ExtTempInput	External Temperature Sensor Input MUX 0x0 : Input connected to PGA 0x1 : Input connected to ADC				
18:15		0x3	ExtTempType	External Temperature Type 0x0 : Reserved 0x1 : Diode/NTC/PTC sink mode, internal bias 0x2 : Diode/NTC/PTC, external bias 0x3 : Diode/NTC/PTC source mode, internal bias 0x4 : Reserved 0x5 : Bridge single ended, internal bias 0x6 : Bridge single ended, external bias 0x7 : Bridge differential				
14:12		0x0	ExtTempAdcShift	ADC Shift V_{Shift} / V_{fs} 0x0 : 0 0x2 : 0.250 0x4 : 0.500 0x6 : 0.750 0x1 : 0.125 0x3 : 0.375 0x5 : 0.625 0x7 : 0.875				
11:8		0x5	ExtTempAdcReso	ADC Resolution 0x0 : 10 Bit 0x2 : 12 Bit 0x4 : 14 Bit 0x1 : 11 Bit 0x3 : 13 Bit 0x5 : 15 Bit				
7		0x0	ExtTempPgaPolarity	PGA Polarity 0x0 : Positive 0x1 : Negative				
6:4		0x0	ExtTempPgaGain2	PGA2 Gain 0x0 : 1.1 0x2 : 1.3 0x4 : 1.5 0x6 : 1.7 0x1 : 1.2 0x3 : 1.4 0x5 : 1.6 0x7 : 1.8				
3:0		0x2	ExtTempPgaGain1	PGA1 Gain 0x0 : 1.2 0x3 : 5.97 0x6 : 29.6 0x9 : 76.6 0xC : 187 0x1 : 2 0x4 : 11.9 0x7 : 39.2 0xA : 112 0xD : 223 0x2 : 4 0x5 : 19.8 0x8 : 58.1 0xB : 143 0xE : 275				

12.4.6 0x1C – ExtTemp3Cfg2

Address : 0x1C		Register Name : ExtTemp3Cfg2		Default: 0x00000010	
Bits	Access	Default	Field Name	Description	
31:14	Reserved	0x0		Reserved	
13:12		0x0	ExtTempSetTime	T1 Input Settling Time before ADC conversion starts 0x0 : 20μs 0x1 : 40μs 0x2 : 60μs 0x3 : 80μs	
11:10		0x0	ExtTempBias	AFE Bias Current Setting 0x0 : normal operation 0x3 : reduced AFE bias current	
9		0x0	ExtTempAdcEnShift	ADC Shift & Gain ×2 Enable, activates BmAdcShift setting 0x0 : ADC Gain ×1, ADC Shift disabled 0x3 : ADC Gain ×2, ADC Shift enabled	
8:5		0x0	ExtTempBrdglBias	Sensor Supply Current, applicable if BmBrdgType = 1 0x0 : Open/Off 0x4 : 40μA 0x8 : 200μA 0x1 : 5μA 0x5 : 80μA 0x9 : 500μA 0x2 : 10μA 0x6 : 100μA 0x3 : 20μA 0x7 : 160μA	
4:0		0x10	ExtTempPgaOffset	PGA Offset Shift 0x1 : -1.9mV 0x10 : 0mV 0x2 : -3.8mV 0x11 : 1.9mV 0x3 : -5.6mV 0x12 : 3.8mV 0x4 : -7.5mV 0x13 : 5.6mV 0x5 : -9.4mV 0x14 : 7.5mV 0x6 : -11.3mV 0x15 : 9.4mV 0x7 : -13.1mV 0x16 : 11.3mV 0x8 : -15.0mV 0x17 : 13.1mV 0x9 : -16.9mV 0x18 : 15.0mV 0xA : -18.8mV 0x19 : 16.9mV 0xB : -20.6mV 0x1A : 18.8mV 0xC : -22.5mV 0x1B : 20.6mV 0xD : -24.4mV 0x1C : 22.5mV 0xE : -26.2mV 0x1D : 24.4mV 0xF : -28.1mV 0x1E : 26.2mV 0x1F : 28.1mV	

12.4.7 0x1D – Cm1Config

Address : 0x1D		Register Name : Cm1Config		Default: 0x0003C004			
Bits	Access	Default	Field Name	Description			
31:20	Reserved	0x0		Reserved			
19		0x0	CmEnShieldDrv	Enable active shield drive 0x0 : Disabled 0x1 : Enabled			
18		0x0	CmEnShift	Enable internal shift cap 0x0 : Disabled 0x1 : Enabled			
17:13		0x1E	CmCapInt	CVC integration capacitance Cint 0x0 : 20 pF 0x8 : 36 pF 0x10 : 52 pF 0x18 : 68 pF 0x1 : 22 pF 0x9 : 38 pF 0x11 : 54 pF 0x19 : 70 pF 0x2 : 24 pF 0xA : 40 pF 0x12 : 56 pF 0x1A : 72 pF 0x3 : 26 pF 0xB : 42 pF 0x13 : 58 pF 0x1B : 74 pF 0x4 : 28 pF 0xC : 44 pF 0x14 : 60 pF 0x1C : 76 pF 0x5 : 30 pF 0xD : 46 pF 0x15 : 62 pF 0x1D : 78 pF 0x6 : 32 pF 0xE : 48 pF 0x16 : 64 pF 0x1E : 80 pF 0x7 : 34 pF 0xF : 50 pF 0x17 : 66 pF 0x1F : 82 pF			
12:8		0x0	CmCapShift	CVC shift capacitance Csh 0x0 : 0 pF 0x8 : 16 pF 0x10 : 32 pF 0x18 : 48 pF 0x1 : 2 pF 0x9 : 18 pF 0x11 : 34 pF 0x19 : 50 pF 0x2 : 4 pF 0xA : 20 pF 0x12 : 36 pF 0x1A : 52 pF 0x3 : 6 pF 0xB : 22 pF 0x13 : 38 pF 0x1B : 54 pF 0x4 : 8 pF 0xC : 24 pF 0x14 : 40 pF 0x1C : 56 pF 0x5 : 10 pF 0xD : 26 pF 0x15 : 42 pF 0x1D : 58 pF 0x6 : 12 pF 0xE : 28 pF 0x16 : 44 pF 0x1E : 60 pF 0x7 : 14 pF 0xF : 30 pF 0x17 : 46 pF 0x1F : 62 pF			
7		0x0	CmAdcEnShift	Enables ADC gain 2x + ADC shift 0x0 : Disabled 0x1 : Enabled			
6:4		0x0	CmAdcShift	ADC Shift 0x0 : 0 0x2 : 0.25 0x4 : 0.5 0x6 : 0.75 0x1 : 0.125 0x3 : 0.375 0x5 : 0.625 0x7 : 0.875			
3:0		0x4	CmAdcReso	ADC Resolution 0x0 : 10 Bit 0x4 : 14 Bit 0x8 : 18 Bit 0xC : 22 Bit 0x1 : 11 Bit 0x5 : 15 Bit 0x9 : 19 Bit 0xD : 23 Bit 0x2 : 12 Bit 0x6 : 16 Bit 0xA : 20 Bit 0xE : 24 Bit 0x3 : 13 Bit 0x7 : 17 Bit 0xB : 21 Bit			

12.4.8 0x1E – Cm2Config

Address : 0x1E		Register Name : Cm2Config		Default: 0x0003C004			
Bits	Access	Default	Field Name	Description			
31:20	Reserved	0x0		Reserved			
19		0x0	CmEnShieldDrv	Enable active shield drive 0x0 : Disabled 0x1 : Enabled			
18		0x0	CmEnShift	Enable internal shift cap 0x0 : Disabled 0x1 : Enabled			
17:13		0x1E	CmCapInt	CVC integration capacitance Cint 0x0 : 20 pF 0x8 : 36 pF 0x10 : 52 pF 0x18 : 68 pF 0x1 : 22 pF 0x9 : 38 pF 0x11 : 54 pF 0x19 : 70 pF 0x2 : 24 pF 0xA : 40 pF 0x12 : 56 pF 0x1A : 72 pF 0x3 : 26 pF 0xB : 42 pF 0x13 : 58 pF 0x1B : 74 pF 0x4 : 28 pF 0xC : 44 pF 0x14 : 60 pF 0x1C : 76 pF 0x5 : 30 pF 0xD : 46 pF 0x15 : 62 pF 0x1D : 78 pF 0x6 : 32 pF 0xE : 48 pF 0x16 : 64 pF 0x1E : 80 pF 0x7 : 34 pF 0xF : 50 pF 0x17 : 66 pF 0x1F : 82 pF			
12:8		0x0	CmCapShift	CVC shift capacitance Csh 0x0 : 0 pF 0x8 : 16 pF 0x10 : 32 pF 0x18 : 48 pF 0x1 : 2 pF 0x9 : 18 pF 0x11 : 34 pF 0x19 : 50 pF 0x2 : 4 pF 0xA : 20 pF 0x12 : 36 pF 0x1A : 52 pF 0x3 : 6 pF 0xB : 22 pF 0x13 : 38 pF 0x1B : 54 pF 0x4 : 8 pF 0xC : 24 pF 0x14 : 40 pF 0x1C : 56 pF 0x5 : 10 pF 0xD : 26 pF 0x15 : 42 pF 0x1D : 58 pF 0x6 : 12 pF 0xE : 28 pF 0x16 : 44 pF 0x1E : 60 pF 0x7 : 14 pF 0xF : 30 pF 0x17 : 46 pF 0x1F : 62 pF			
7		0x0	CmAdcEnShift	Enables ADC gain 2x + ADC shift 0x0 : Disabled 0x1 : Enabled			
6:4		0x0	CmAdcShift	ADC Shift 0x0 : 0 0x2 : 0.25 0x4 : 0.5 0x6 : 0.75 0x1 : 0.125 0x3 : 0.375 0x5 : 0.625 0x7 : 0.875			
3:0		0x4	CmAdcReso	ADC Resolution 0x0 : 10 Bit 0x4 : 14 Bit 0x8 : 18 Bit 0xC : 22 Bit 0x1 : 11 Bit 0x5 : 15 Bit 0x9 : 19 Bit 0xD : 23 Bit 0x2 : 12 Bit 0x6 : 16 Bit 0xA : 20 Bit 0xE : 24 Bit 0x3 : 13 Bit 0x7 : 17 Bit 0xB : 21 Bit			

12.4.9 0x1F – CmConfig

Address : 0x1F		Register Name : CmConfig		Default: 0x00000000			
Bits	Access	Default	Field Name	Description			
31:10	Reserved	0x0		Reserved			
9		0x0	CMShieldDrv10nF	Enable 10nF shield driver mode 0x0 : Disabled 0x1 : Enabled			
8		0x0	CmNoiseMode	Noise Mode 0x0 : Normal 0x1 : Low Noise			
7		0x0	CmEnRatio	Enable difference measurement mode 0x0 : Disabled 0x1 : Enabled			
6:2		0x0	CmRefSel				
1		0x0	CmEnDiff	Enable ratiometric measurement mode 0x0 : Disabled 0x1 : Enabled			
0		0x0	CmSenseCapType	Input capacitor type 0x0 : Isolated 0x1 : Grounded			

12.5 PTAT Sensor

12.5.1 0x20 – PtatCfg1

Address : 0x20		Register Name : PtatCfg1		Default: 0x0000F533				
Bits	Access	Default	Field Name	Description				
31:18	Reserved	0x0		Reserved				
17:15		0x1	AdcMux	ADC Input MUX Setting 0x1 : ADC input connected to PGA ¹				
14:12		0x7	AdcShift	ADC Shift V _{Shift} / V _{fs} 0x0 : 0 0x2 : 0.250 0x4 : 0.500 0x6 : 0.750 0x1 : 0.125 0x3 : 0.375 0x5 : 0.625 0x7 : 0.875 ¹				
11:8		0x5	AdcReso	ADC Resolution 0x0 : 10 Bit 0x2 : 12 Bit 0x4 : 14 Bit 0x1 : 11 Bit 0x3 : 13 Bit 0x5 : 15 Bit				
7		0x0	PgaPolarity	PGA Polarity 0x0 : Positive ¹ 0x1 : Negative				
6:4		0x3	PgaGain2	PGA2 Gain 0x0 : 1.1 0x2 : 1.3 0x4 : 1.5 0x6 : 1.7 0x1 : 1.2 0x3 : 1.4 ¹ 0x5 : 1.6 0x7 : 1.8				
3:0		0x3	PgaGain1	PGA1 Gain 0x0 : 1.2 0x3 : 5.97 ¹ 0x6 : 29.6 0x9 : 76.6 0xC : 187 0x1 : 2 0x4 : 11.9 0x7 : 39.2 0xA : 112 0xD : 223 0x2 : 4 0x5 : 19.8 0x8 : 58.1 0xB : 143 0xE : 275				

¹ Renesas recommended

12.5.2 0x21 – PtatCfg2

Address : 0x21		Register Name : PtatCfg2		Default: 0x00000030	
Bits	Access	Default	Field Name	Description	
31:8	Reserved	0x0		Reserved	
7:6		0x0	Bias	AFE Bias Current Setting 0x0 : normal operation 0x3 : reduced AFE bias current	
5		0x1	AdcEnShift	ADC Shift & Gain ×2 Enable, activates AdcShift setting 0x0 : ADC Gain ×1, ADC Shift disabled 0x3 : ADC Gain ×2, ADC Shift enabled ¹	
4:0		0x10	PgaOffset	PGA Offset Shift 0x1 : -1.9mV 0x10 : 0mV ¹ 0x2 : -3.8mV 0x11 : 1.9mV 0x3 : -5.6mV 0x12 : 3.8mV 0x4 : -7.5mV 0x13 : 5.6mV 0x5 : -9.4mV 0x14 : 7.5mV 0x6 : -11.3mV 0x15 : 9.4mV 0x7 : -13.1mV 0x16 : 11.3mV 0x8 : -15.0mV 0x17 : 13.1mV 0x9 : -16.9mV 0x18 : 15.0mV 0xA : -18.8mV 0x19 : 16.9mV 0xB : -20.6mV 0x1A : 18.8mV 0xC : -22.5mV 0x1B : 20.6mV 0xD : -24.4mV 0x1C : 22.5mV 0xE : -26.2mV 0x1D : 24.4mV 0xF : -28.1mV 0x1E : 26.2mV 0x1F : 28.1mV	

¹ Renesas recommended

12.6 AFE Sequencer

12.6.1 0x22 – Afe1MeasCfg1

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x22		Register Name : Afe1MeasCfg1		Default: 0x01020036
Bits	Access	Default	Field Name	Description
31		0x0	BurstModeSlot8	AFE DMA Burst Mode Data Transfer after Slot_x 0x0 : Disabled 0x1 : Enabled
30		0x0	BurstModeSlot7	
29		0x0	BurstModeSlot6	
28		0x0	BurstModeSlot5	
27		0x0	BurstModeSlot4	
26		0x0	BurstModeSlot3	
25		0x0	BurstModeSlot2	
24		0x1	BurstModeSlot1	
23		0x0	EocIrqSlot8	End of Conversion Interrupt after Slot_x 0x0 : Disabled 0x1 : Enabled
22		0x0	EocIrqSlot7	
21		0x0	EocIrqSlot6	
20		0x0	EocIrqSlot5	
19		0x0	EocIrqSlot4	
18		0x0	EocIrqSlot3	
17		0x1	EocIrqSlot2	
16		0x0	EocIrqSlot1	
15:14		0x0	MeasTypeSlot8	AFE Measurement Type for Slot_x 0x0 : None 0x1 : SM- 0x2 : SM+ 0x3 : AUX_i
13:12		0x0	MeasTypeSlot7	
11:10		0x0	MeasTypeSlot6	
9:8		0x0	MeasTypeSlot5	
7:6		0x0	MeasTypeSlot4	
5:4		0x3	MeasTypeSlot3	
3:2		0x1	MeasTypeSlot2	
1:0		0x2	MeasTypeSlot1	

12.6.2 0x23 – Afe1MeasCfg2

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x23		Register Name : Afe1MeasCfg2		Default: 0x00000013
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:8		0x0	AuxMaxTime	Maximum lenght of AUX_i measurement slots within a sequence 0x0000 ... 0xFFFF AFE clock cycles The parameter is calculated based on the relevant timing setups of all active AUX_i measurements to secure all AUX_i measurements have the same duration. This is mainly required for synchronized AFE operation.
7:6		0x0	AuxInsertRate	Insertion Rate of an AUX_i measurement in „Accelerated main measurement“ setup 0x0 : Disabled 0x1 : Every 2nd 0x2 : Every 4th 0x3 : Every 8th
5:4		0x1	CyclicMode	Sequencer Run Mode 0x0 : Single measurement 0x1 : Continuous cyclic measurement 0x2 : Discontinuous cyclic measurement, started by trigger
3:0		0x3	NrOfSlots	Number of active measurement slots 0x0 ... 0x8 selectable

12.6.3 0x24 – Afe1MeasCfg3

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x24			Register Name : Afe1MeasCfg3		Default: 0x00000018
Bits	Access	Default	Field Name	Description	
31	Reserved	0x0	AuxMeasEnable0Aux32	Activation of Auxiliary measurements Bit 0 : Auto-zero (AZ) measurement on Sensor Bridge Bit 1 : PTAT Sensor S- Bit 2 : PTAT Sensor S+ Bit 3 : T1 Sensor S- Bit 4 : T1 Sensor S+ Bit 5 : T1 Sensor, check short to top Bit 6 : T1 Sensor, check short to bottom Bit 7 : T1 Sensor, check open Bit 8 : T2 Sensor S- Bit 9 : T2 Sensor S+ Bit 10 : T2 Sensor, check short to top Bit 11 : T2 Sensor, check short to bottom Bit 12 : T2 Sensor, check open Bit 13 : T3 Sensor S- Bit 14 : T3 Sensor S+ Bit 15 : T3 Sensor, check short to top Bit 16 : T3 Sensor, check short to bottom Bit 17 : T3 Sensor, check open Bit 18 : AFE gain diagnosis S+ Bit 19 : AFE gain diagnosis S- Bit 22 : AFE offset diagnosis Bit 27 : Bridge Sensor connection check, INP or INN open Bit 28 : Bridge Sensor connection check, INP and INN shorted	
30	Reserved	0x0	AuxMeasEnable0Aux31		
29	Reserved	0x0	AuxMeasEnable0Aux30		
28		0x0	AuxMeasEnable0Aux29		
27		0x0	AuxMeasEnable0Aux28		
26		0x0	AuxMeasEnable0Aux27		
25		0x0	AuxMeasEnable0Aux26		
24		0x0	AuxMeasEnable0Aux25		
23		0x0	AuxMeasEnable0Aux24		
22		0x0	AuxMeasEnable0Aux23		
21		0x0	AuxMeasEnable0Aux22		
20		0x0	AuxMeasEnable0Aux21		
19		0x0	AuxMeasEnable0Aux20		
18		0x0	AuxMeasEnable0Aux19		
17		0x0	AuxMeasEnable0Aux18		
16		0x0	AuxMeasEnable0Aux17		
15		0x0	AuxMeasEnable0Aux16		
14		0x0	AuxMeasEnable0Aux15		
13		0x0	AuxMeasEnable0Aux14		
12		0x0	AuxMeasEnable0Aux13		
11		0x0	AuxMeasEnable0Aux12		
10		0x0	AuxMeasEnable0Aux11		
9		0x0	AuxMeasEnable0Aux10		
8		0x0	AuxMeasEnable0Aux9		
7		0x0	AuxMeasEnable0Aux8		
6		0x0	AuxMeasEnable0Aux7		
5		0x0	AuxMeasEnable0Aux6		
4		0x1	AuxMeasEnable0Aux5		
3		0x1	AuxMeasEnable0Aux4		
2		0x0	AuxMeasEnable0Aux3		
1		0x0	AuxMeasEnable0Aux2		
0		0x0	AuxMeasEnable0Aux1		
				All other bits reserved	
				Bit Value Meaning	
				0 : Aux measurement Skipped	
				1 : Aux measurement Executed	

12.6.4 0x25 – Afe1MeasCfg4

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x25		Register Name : Afe1MeasCfg4		Default: 0x00400000
Bits	Access	Default	Field Name	Description
31:25	Reserved	0x0		Reserved
24		0x0	SensBufDepth	Bridge Sensor data buffer depth in SRAM 0x0 : data buffer depth 1 0x1 : data buffer depth 8
23		0x0	IrqEnableEoauxaz	End of AZ Measurement 0x0 : IRQ disabled 0x1 : IRQ enabled
22		0x1	IrqEnableEoauxseq	End of Aux Sequence 0x0 : IRQ disabled 0x1 : IRQ enabled
21		0x0	IrqEnableEoauxins	End of Inserted AUX Measurement 0x0 : IRQ disabled 0x1 : IRQ enabled
20:5		0x0	IdleTime	In continuous cyclic measurement mode idle times up to 10ms can be asserted between two sequences. IdleTime represents a number of AFE clocks – 4MHz by default
4	Reserved	0x0	AuxMeasEnable1Aux37	Enable CVC diagnosis leak_2 S+
3	Reserved	0x0	AuxMeasEnable1Aux36	Enable CVC diagnosis leak_2 S-
2	Reserved	0x0	AuxMeasEnable1Aux35	Enable CVC diagnosis leak_1 S+
1	Reserved	0x0	AuxMeasEnable1Aux34	Enable CVC diagnosis leak_1 S-
0	Reserved	0x0	AuxMeasEnable1Aux33	Enable sensor leakage check P

12.6.5 0x26 – Afe2MeasCfg1

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x26		Register Name : Afe2MeasCfg1		Default: 0x01020036
Bits	Access	Default	Field Name	Description
31		0x0	BurstModeSlot8	AFE DMA Burst Mode Data Transfer after Slot_x 0x0 : Disabled 0x1 : Enabled
30		0x0	BurstModeSlot7	
29		0x0	BurstModeSlot6	
28		0x0	BurstModeSlot5	
27		0x0	BurstModeSlot4	
26		0x0	BurstModeSlot3	
25		0x0	BurstModeSlot2	
24		0x1	BurstModeSlot1	
23		0x0	EocIrqSlot8	End of Conversion Interrupt after Slot_x 0x0 : Disabled 0x1 : Enabled
22		0x0	EocIrqSlot7	
21		0x0	EocIrqSlot6	
20		0x0	EocIrqSlot5	
19		0x0	EocIrqSlot4	
18		0x0	EocIrqSlot3	
17		0x1	EocIrqSlot2	
16		0x0	EocIrqSlot1	
15:14		0x0	MeasTypeSlot8	AFE Measurement Type for Slot_x 0x0 : None 0x1 : SM- 0x2 : SM+ 0x3 : AUX_i
13:12		0x0	MeasTypeSlot7	
11:10		0x0	MeasTypeSlot6	
9:8		0x0	MeasTypeSlot5	
7:6		0x0	MeasTypeSlot4	
5:4		0x3	MeasTypeSlot3	
3:2		0x1	MeasTypeSlot2	
1:0		0x2	MeasTypeSlot1	

12.6.6 0x27 – Afe2MeasCfg2

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x27		Register Name : Afe2MeasCfg2		Default: 0x00000013
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:8		0x0	AuxMaxTime	Maximum lenght of AUX_i measurement slots within a sequence 0x0000 ... 0xFFFF AFE clock cycles The parameter is calculated based on the relevant timing setups of all active AUX_i measurements to secure all AUX_i measurements have the same duration. This is mainly required for synchronized AFE operation.
7:6		0x0	AuxInsertRate	Insertion Rate of an AUX_i measurement in „Accelerated main measurement“ setup 0x0 : Disabled 0x1 : Every 2nd 0x2 : Every 4th 0x3 : Every 8th
5:4		0x1	CyclicMode	Sequencer Run Mode 0x0 : Single measurement 0x1 : Continuous cyclic measurement 0x2 : Discontinuous cyclic measurement, started by trigger
3:0		0x3	NrOfSlots	Number of active measurement slots 0x0 ... 0x8 selectable

12.6.7 0x28 – Afe2MeasCfg3

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x28			Register Name : Afe2MeasCfg3	Default: 0x00000300
Bits	Access	Default	Field Name	Description
31	Reserved	0x0	AuxMeasEnable0Aux32	Activation of Auxiliary measurements Bit 0 : Auto-zero (AZ) measurement on Sensor Bridge Bit 1 : PTAT Sensor S- Bit 2 : PTAT Sensor S+ Bit 3 : T1 Sensor S- Bit 4 : T1 Sensor S+ Bit 5 : T1 Sensor, check short to top Bit 6 : T1 Sensor, check short to bottom Bit 7 : T1 Sensor, check open Bit 8 : T2 Sensor S- Bit 9 : T2 Sensor S+ Bit 10 : T2 Sensor, check short to top Bit 11 : T2 Sensor, check short to bottom Bit 12 : T2 Sensor, check open Bit 13 : T3 Sensor S- Bit 14 : T3 Sensor S+ Bit 15 : T3 Sensor, check short to top Bit 16 : T3 Sensor, check short to bottom Bit 17 : T3 Sensor, check open Bit 18 : AFE gain diagnosis S+ Bit 19 : AFE gain diagnosis S- Bit 22 : AFE offset diagnosis Bit 27 : Bridge Sensor connection check, INP or INN open Bit 28 : Bridge Sensor connection check, INP and INN shorted
30	Reserved	0x0	AuxMeasEnable0Aux31	
29	Reserved	0x0	AuxMeasEnable0Aux30	
28		0x0	AuxMeasEnable0Aux29	
27		0x0	AuxMeasEnable0Aux28	
26		0x0	AuxMeasEnable0Aux27	
25		0x0	AuxMeasEnable0Aux26	
24		0x0	AuxMeasEnable0Aux25	
23		0x0	AuxMeasEnable0Aux24	
22		0x0	AuxMeasEnable0Aux23	
21		0x0	AuxMeasEnable0Aux22	
20		0x0	AuxMeasEnable0Aux21	
19		0x0	AuxMeasEnable0Aux20	
18		0x0	AuxMeasEnable0Aux19	
17		0x0	AuxMeasEnable0Aux18	
16		0x0	AuxMeasEnable0Aux17	
15		0x0	AuxMeasEnable0Aux16	
14		0x0	AuxMeasEnable0Aux15	
13		0x0	AuxMeasEnable0Aux14	
12		0x0	AuxMeasEnable0Aux13	
11		0x0	AuxMeasEnable0Aux12	
10		0x0	AuxMeasEnable0Aux11	
9		0x1	AuxMeasEnable0Aux10	
8		0x1	AuxMeasEnable0Aux9	
7		0x0	AuxMeasEnable0Aux8	
6		0x0	AuxMeasEnable0Aux7	
5		0x0	AuxMeasEnable0Aux6	
4		0x0	AuxMeasEnable0Aux5	
3		0x0	AuxMeasEnable0Aux4	
2		0x0	AuxMeasEnable0Aux3	
1		0x0	AuxMeasEnable0Aux2	
0		0x0	AuxMeasEnable0Aux1	
				All other bits reserved
				Bit Value Meaning
				0 : Aux measurement Skipped
				1 : Aux measurement Executed

12.6.8 0x29 – Afe2MeasCfg4

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x29		Register Name : Afe2MeasCfg4		Default: 0x00400000
Bits	Access	Default	Field Name	Description
31:25	Reserved	0x0		Reserved
24		0x0	SensBufDepth	Bridge Sensor data buffer depth in SRAM 0x0 : data buffer depth 1 0x1 : data buffer depth 8
23		0x0	IrqEnableEoauxaz	End of AZ Measurement 0x0 : IRQ disabled 0x1 : IRQ enabled
22		0x1	IrqEnableEoauxseq	End of Aux Sequence 0x0 : IRQ disabled 0x1 : IRQ enabled
21		0x0	IrqEnableEoauxins	End of Inserted AUX Measurement 0x0 : IRQ disabled 0x1 : IRQ enabled
20:5		0x0	IdleTime	In continuous cyclic measurement mode idle times up to 10ms can be asserted between two sequences. IdleTime represents a number of AFE clocks – 4MHz by default
4	Reserved	0x0	AuxMeasEnable1Aux37	Enable CVC diagnosis leak_2 S+
3	Reserved	0x0	AuxMeasEnable1Aux36	Enable CVC diagnosis leak_2 S-
2	Reserved	0x0	AuxMeasEnable1Aux35	Enable CVC diagnosis leak_1 S+
1	Reserved	0x0	AuxMeasEnable1Aux34	Enable CVC diagnosis leak_1 S-
0	Reserved	0x0	AuxMeasEnable1Aux33	Enable sensor leakage check P

12.7 Diagnosis

12.7.1 0x2A – DiagSen.DiagCfg

Address : 0x2A		Register Name : DiagSen.DiagCfg		Default: 0x10000000
Bits	Access	Default	Field Name	Description
31:29	Reserved	0x0		Reserved
28:24		0x10	LeakTolVal	The Leakage Tolerance Register Value can be calculated like this: Register Value = $(2^5 - 1) * \text{LeakTol} / 100$
23:17	Reserved	0x0		Reserved
16:15		0x0	Extt3Range	Reference for Temp Sensor open check on T3 0x0 : 2MΩ 0x1 : 0.5MΩ 0x3 : 0.1MΩ
14		0x0	Extt3Pt100	Reference for temperature sensor short measurement on T3 0x0 : RT_SHORT < 500Ω 0x1 : RT_SHORT < 10Ω
13	Reserved	0x0		Reserved
12:11		0x0	Extt2Range	Reference for Temp Sensor open check on T2 0x0 : 2MΩ 0x1 : 0.5MΩ 0x3 : 0.1MΩ
10		0x0	Extt2Pt100	Reference for temperature sensor short measurement on T2 0x0 : RT_SHORT < 500Ω 0x1 : RT_SHORT < 10Ω
9	Reserved	0x0		Reserved
8:7		0x0	Extt1Range	Reference for Temp Sensor open check on T1 0x0 : 2MΩ 0x1 : 0.5MΩ 0x3 : 0.1MΩ
6		0x0	Extt1Pt100	Reference for temperature sensor short measurement on T1 0x0 : RT_SHORT < 500Ω 0x1 : RT_SHORT < 10Ω
5:4		0x0	Afe2GainChkResDacVal	Resistive Diagnosis DAC value at AFE2 0x0 : 2mV 0x1 : 10mV 0x2 : 100mV 0x3 : 200mV
3		0x0	Afe2GainChkResDacEn	Resistive Diagnosis DAC activation at AFE2 0x0 : Disabled 0x1 : Enabled
2:1		0x0	Afe1GainChkResDacVal	Resistive Diagnosis DAC value at AFE1 0x0 : 2mV 0x1 : 10mV 0x2 : 100mV 0x3 : 200mV
0		0x0	Afe1GainChkResDacEn	Resistive Diagnosis DAC activation at AFE1 0x0 : Disabled 0x1 : Enabled

12.7.2 0x2B – DiagSen.Range[0].Inp

Address : 0x2B		Register Name : DiagSen.Range[0].Inp		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:16		0x0	Max	
15:0		0x0	Min	

12.7.3 0x2C – DiagSen.Range[0].Inn

Address : 0x2C		Register Name : DiagSen.Range[0].Inn		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:16		0x0	Max	
15:0		0x0	Min	

12.7.4 0x2D – DiagSen.Range[1].Inp

Address : 0x2D		Register Name : DiagSen.Range[1].Inp		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:16		0x0	Max	
15:0		0x0	Min	

12.7.5 0x2E – DiagSen.Range[1].Inn

Address : 0x2E		Register Name : DiagSen.Range[1].Inn		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:16		0x0	Max	
15:0		0x0	Min	

12.7.6 0x2F – DiagSen.GainChk[0]

Address : 0x2F		Register Name : DiagSen.GainChk[0]		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:16		0x0	TolVal	Gain Tolerance Value for Gain Drift Diagnosis A tolerance value in ADC counts for acceptable gain drift over lifetime shall be stored in this register A gain failure is signaled after the Gain Drift Check if the determined AFE Gain Value is either < (RefVal - TolVal) or > (RefVal + TolVal)
15:0		0x0	RefVal	Gain Reference Value for Gain Drift Diagnosis During sensor calibration an initial AFE Gain Check measurement with a properly defined AFExGainCheckResDacVal setting must be done and the obtained RAW output value shall be stored in this register for later reference.

12.7.7 0x30 – DiagSen.GainChk[1]

Address : 0x30		Register Name : DiagSen.GainChk[1]		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:16		0x0	TolVal	
15:0		0x0	RefVal	

12.7.8 0x31 – DiagSen.OfstChk[0]

Address : 0x31		Register Name : DiagSen.OfstChk[0]		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:16		0x0	TolVal	
15:0		0x0	RefVal	

12.7.9 0x32 – DiagSen.OfstChk[1]

Address : 0x32		Register Name : DiagSen.OfstChk[1]		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:16		0x0	TolVal	
15:0		0x0	RefVal	

12.8 Temperature Channel Mapping

12.8.1 0x33 – TempMapChId

Address : 0x33		Register Name : TempMapChId		Default: 0x0000001A
Bits	Access	Default	Field Name	Description
31:9	Reserved	0x0		Reserved
8:6		0x0	Tch3	Temperature Sensor Source for Temperature Channels 1, 2, 3 0x0 : None 0x1 : PTAT 0x2 : T1 0x3 : T2 0x4 : T3
5:3		0x3	Tch2	
2:0		0x2	Tch1	

12.9 SSC Algorithm Selection

12.9.1 0x34 – MathSbrAlgoSel

Address : 0x34		Register Name : MathSbrAlgoSel		Default: 0x04040011
Bits	Access	Default	Field Name	Description
31	Reserved	0x0		Reserved
30:24		0x4	DigGain2	Digital gain 1 0x0 : 0 0x1 : 0.25 0x2 : 0.5 ... 0x1F : 7.75 0x20 : 8 ... 0x7C : 31
23	Reserved	0x0		Reserved
22:16		0x4	DigGain1	Digital gain 2 0x0 : 0 0x1 : 0.25 0x2 : 0.5 ... 0x1F : 7.75 0x20 : 8 ... 0x7C : 31
15:12	Reserved	0x0		Reserved
11		0x0	TlcChOrder	Third Logic Channel Operand Order 0x0 : CH1 op CH2 0x1 : CH2 op CH1
10:8		0x0	TlcOp	Third Logic Channel Operation 0x0 : Subtraction 0x1 : Division 0x2 : Ratio
7:4		0x1	Sensor2	SSC Algorithm for Bridge Sensors 1 & 2 0x0 : None 0x1 : SOT Parabolic 0x2 : SOT S-Shaped
3:0		0x1	Sensor1	

12.10 EOC / Alarm

12.10.1 0x35 – EocAlarmPin[0].Reg1

Address : 0x35		Register Name : EocAlarmPin[0].Reg1		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:29	Reserved	0x0		Reserved
28		0x0	Range	Alarm Range 0x0 : Above / Outside 0x1 : Below / Inside
27:26		0x0	NrThresh	Number of Alarm Thresholds 0x0 : None (EOC Mode) 0x1 : Enabled 0x2 : Window (2 Thresholds)
25		0x0	Pol	Output Polarity 0x0 : Active High 0x1 : Active Low
24		0x0	En	EOC / Alarm Activation 0x0 : Disabled 0x1 : Enabled
23:0		0x0	Thresh1	Alarm Threshold 1 24 bit value, matches SSC output number format

12.10.2 0x36 – EocAlarmPin[0].Reg2

Address : 0x36		Register Name : EocAlarmPin[0].Reg2		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	Thresh2	Alarm Threshold 2 24 bit value, matches SSC output number format

12.10.3 0x37 – EocAlarmPin[0].Reg3

Address : 0x37		Register Name : EocAlarmPin[0].Reg3		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24		0x0	Persist	
23:0		0x0	Hyst	Alarm Hysteresis 24bit value, matches SSC output number format

12.10.4 0x38 – EocAlarmPin[1].Reg1

Address : 0x38		Register Name : EocAlarmPin[1].Reg1		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:29	Reserved	0x0		Reserved
28		0x0	Range	Alarm Range 0x0 : Above / Outside 0x1 : Below / Inside
27:26		0x0	NrThresh	Number of Alarm Thresholds 0x0 : None (EOC Mode) 0x1 : Enabled 0x2 : Window (2 Thresholds)
25		0x0	Pol	Output Polarity 0x0 : Active High 0x1 : Active Low
24		0x0	En	EOC / Alarm Activation 0x0 : Disabled 0x1 : Enabled
23:0		0x0	Thresh1	Alarm Threshold 1 24 bit value, matches SSC output number format

12.10.5 0x39 – EocAlarmPin[1].Reg2

Address : 0x39		Register Name : EocAlarmPin[1].Reg2		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	Thresh2	Alarm Threshold 2 24 bit value, matches SSC output number format

12.10.6 0x3A – EocAlarmPin[1].Reg3

Address : 0x3A		Register Name : EocAlarmPin[1].Reg3		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24		0x0	Persist	Alarm Condition Persistence before Alarm State is changed 8bit value (0 ... 255)
23:0		0x0	Hyst	

12.11 Analog Output (AOUT)

12.11.1 0x3B – AoutSelParam

Address : 0x3B		Register Name : AoutSelParam		Default: 0x00000001
Bits	Access	Default	Field Name	Description
31:7	Reserved	0x0		Reserved
6:3		0x0	AoutModSel	Analog Output Driver Mode 0x0 : Disabled 0x1 : Absolute Voltage Output 0-10V 0x2 : Absolute Voltage Output 0-5V 0x3 : Absolute V 0-1V 0x4 : Ratiometric Voltage Output 0x5 : 2-Wire Current Loop 0x6 : 3-Wire Current Loop 0x7 : Auto-Detect Current Loop
2:0		0x1	SelAfeForDac	Source Signal for Analog Output 0x0 : None 0x1 : Bridge Sensor Channel 1 0x2 : Bridge Sensor Channel 2 0x3 : Third Logic Channel 0x4 : Temperature Channel 1 0x5 : Temperature Channel 2 0x6 : Temperature Channel 3

12.11.2 0x3C – AoutRegCtrl

Address : 0x3C		Register Name : AoutRegCtrl		Default: 0x0000001A	
Bits	Access	Default	Field Name	Description	
31:13	Reserved	0x0		Reserved	
12:11		0x0	Aout5vRdacRefSel		
10:9		0x0	AoutVddnLoad	VDDN Charge Pump Load Current 0x0 : 0.5mA 0x2 : 3mA 0x1 : 1mA 0x3 : 5mA	
8		0x0	AoutVddnEn	VDDN Charge Pump for Negative Supply 0x0 : Disabled 0x1 : Enabled	
7		0x0	AoutOffsetCompOff	Analog Output Offset Compensation 0x0 : Disabled 0x1 : Enabled	
6:5		0x0	AoutCurrLim	Analog Driver Output Current Limitation 0x0 : 6mA 0x2 : 18mA 0x1 : 12mA 0x3 : 25mA	
4		0x1	AoutFeedBackEn	Analog Driver Feedback 0x0 : External 0x1 : Internal	
3		0x1	AoutHighPowEn	Analog Driver Output Power 0x0 : Low Power 0x1 : High Power	
2:1		0x1	AoutMode	Analog Output Mode 0x0 : Current Loop 5V-RDAC 0x1 : VOUT 5V 0x2 : VOUT 1V 0x3 : Current Loop 1V-RDAC	
0		0x0	AoutEn	Analog Output Activation 0x0 : Disabled 0x1 : Enabled	

12.11.3 0x3D – AoutRegDiag

Address : 0x3D		Register Name : AoutRegDiag		Default: 0x00000000	
Bits	Access	Default	Field Name	Description	
31:4	Reserved	0x0		Reserved	
3		0x0	AoutDiagVddaEn	VDDA Diagnosis if VDDA regulator for AOUT is turned on 0x0 : Disabled 0x1 : Enabled	
2:1		0x0	AoutDiagOutValue	Analog Output Mode 0x0 : V _{AOUT} = VSS 0x2 : V _{AOUT} = 96%VDD 0x1 : V _{AOUT} = 5% VDD 0x3 : V _{AOUT} = VDD	
0		0x0	AoutDiagOutEn	Diagnosis Level Output at AOUT 0x0 : Normal Operation Mode 0x1 : Diagnosis Output Mode	

12.11.4 0x3E – AoutCl2Coeff

Address : 0x3E		Register Name : AoutCl2Coeff		Default: 0x00000000	
Bits	Access	Default	Field Name	Description	
31:16		0x0	ClDelta	2-Wire Current Loop Calibration Coefficient CL2_Delta 16-bit Value	
15:0		0x0	ClOffset	2-Wire Current Loop Calibration Coefficient CL2_Offset 16-bit Value	

12.11.5 0x3F – AoutCl3Coeff

Address : 0x3F		Register Name : AoutCl3Coeff		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:16		0x0	ClDelta	3-Wire Current Loop Calibration Coefficient CL3_Delta 16-bit Value
15:0		0x0	ClOffset	3-Wire Current Loop Calibration Coefficient CL3_Offset 16-bit Value

12.12 System Startup

12.12.1 0x40 – StartupParamCfg

Address : 0x40		Register Name : StartupParamCfg		Default: 0x00000001
Bits	Access	Default	Field Name	Description
31:9	Reserved	0x0		Reserved
8		0x0	EobEn	End of Busy Enable 0x0 : Disabled 0x1 : Enabled
7:2	Reserved	0x0		Reserved
1:0		0x1	StartupMode	System Startup Mode 0x0 : Cyclic Mode 0x1 : Command Mode

12.13 IIR Filter

12.13.1 0x41 – IirFiltCoeffReg

Address : 0x41		Register Name : IirFiltCoeffReg		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:30	Reserved	0x0		Reserved
29:27		0x0	FiltTemp3Diff	IIR Diff Value Temperature Channel 3
26:24		0x0	FiltTemp3Avg	IIR Avg Value Temperature Channel 3
23:21		0x0	FiltTemp2Diff	IIR Diff Value Temperature Channel 2
20:18		0x0	FiltTemp2Avg	IIR Avg Value Temperature Channel 2
17:15		0x0	FiltTemp1Diff	IIR Diff Value Temperature Channel 1
14:12		0x0	FiltTemp1Avg	IIR Avg Value Temperature Channel 1
11:9		0x0	FiltSbr2Diff	IIR Diff Value Sensor Bridge 2
8:6		0x0	FiltSbr2Avg	IIR Avg Value Sensor Bridge 2
5:3		0x0	FiltSbr1Diff	IIR Diff Value Sensor Bridge 1
2:0		0x0	FiltSbr1Avg	IIR Avg Value Sensor Bridge 1

12.14 General AFE Configuration

12.14.1 0x42 – AfeConfig

Address : 0x42		Register Name : AfeConfig		Default: 0x20000000	
Bits	Access	Default	Field Name	Description	
31		0x0	CLMode	AFE Operation Mode for 2-Wire Current Loop application 0x0 : Disabled 0x1 : Enabled	
30:26	Reserved	0x8	AfeMisc	Reserved	
25		0x0	Afe2LowSpeed	AFE2 clock speed with respect to AFE1 0x0 : Normal (equal) Speed 0x1 : Quarter Speed	
24	Reserved	0x0	CM2En	Reserved	
23	Reserved	0x0	CM1En	Reserved	
22		0x0	Vdda3Brownout	AOUT Vdda Brownout Diagnosis 0x0 : Disabled 0x1 : Enabled	
21		0x0	Vdda2Brownout	AFE2 Vdda Brownout Diagnosis 0x0 : Disabled 0x1 : Enabled	
20		0x0	Vdda1Brownout	AFE1 Vdda Brownout Diagnosis 0x0 : Disabled 0x1 : Enabled	
19	Reserved	0x0	CMDitheringEnable	Reserved	
18	Reserved	0x0	CMNoiseInt1	Reserved	
17		0x0	TNoiseInt1	ADC 10μV Noise Reduction 0x0 : Disabled 0x1 : Enabled	
16		0x0	ExtTemp3NoiseInt1		
15		0x0	ExtTemp2NoiseInt1		
14		0x0	ExtTemp1NoiseInt1		
13		0x0	BM2NoiseInt1		
12		0x0	BM1NoiseInt1		
11:10		0x0	TChpMode	PGA Chopper Mode PTAT Temperature Sensor 0x0 : 100kHz 0x2 : 50kHz 0x1 : 200kHz 0x3 : Chopper Off	
9:8		0x0	ExtTemp3ChpMode	PGA Chopper Mode External Temperature Sensor T3 0x0 : 100kHz 0x2 : 50kHz 0x1 : 200kHz 0x3 : Chopper Off	
7:6		0x0	ExtTemp2ChpMode	PGA Chopper Mode External Temperature Sensor T2 0x0 : 100kHz 0x2 : 50kHz 0x1 : 200kHz 0x3 : Chopper Off	
5:4		0x0	ExtTemp1ChpMode	PGA Chopper Mode External Temperature Sensor T1 0x0 : 100kHz 0x2 : 50kHz 0x1 : 200kHz 0x3 : Chopper Off	
3:2		0x0	BM2ChpMode	PGA Chopper Mode Bridge Sensor 2 0x0 : 100kHz 0x2 : 50kHz 0x1 : 200kHz 0x3 : Chopper Off	
1:0		0x0	BM1ChpMode	PGA Chopper Mode Bridge Sensor 1 0x0 : 100kHz 0x2 : 50kHz 0x1 : 200kHz 0x3 : Chopper Off	

12.15 Output Modulation

12.15.1 0x43 – OutModConf

Address : 0x43		Register Name : OutModConf		Default: 0x27106400
Bits	Access	Default	Field Name	Description
31:16		0x2710	FmMaxFreqPwmBaseFreq	Frequency Modulation - Maximum Frequency in Hz 16bit value in range 1,000 to 10,000 Pulse Width Modulation - PWM Mapping Selects if the conditioned result is inverted. 0x0 : 200 Hz 0x1 : 500 Hz 0x2 : 500Hz + 1 * 500Hz = 1kHz 0x3 : 500Hz + 2 * 500Hz = 1kHz 0x4...31 : 500Hz + (FmMinFreqPwmMap-1) * 500Hz 0x32 : 500Hz + 31 * 500Hz = 15kHz
15:8		0x64	FmMinFreqPwmMap	Frequency Modulation - Minimum Frequency in Hz 8bit value in range 100 to 255 Pulse Width Modulation - PWM Mapping Selects if the conditioned result is inverted. 0x0 : SSCMax = 100% and SSCMin = 0% 0x1 : SSCMax = 0% and SSCMin = 100%
7:5		0x0	ChGpio7	Source Signal for FOUT/PWM_2 0x0 : Not Used 0x1 : Bridge Sensor 1 0x2 : Bridge Sensor 2 0x3 : Third Logic Channel 0x4 : Temperature Channel 1 0x5 : Temperature Channel 2 0x6 : Temperature Channel 3
4:2		0x0	ChGpio1	Source Signal for FOUT/PWM_1 0x0 : Not Used 0x1 : Bridge Sensor 1 0x2 : Bridge Sensor 2 0x3 : Third Logic Channel 0x4 : Temperature Channel 1 0x5 : Temperature Channel 2 0x6 : Temperature Channel 3
1:0		0x0	Sel	Output Modulation Type 0x0 : No Output Modulation 0x1 : Frequency Modulation 0x2 : Pulse Width Modulation

12.16 Output Clipping, Diagnostic Range Assignment and Watchdog

12.16.1 0x44 – DiagClipOutCfg.SysDiagCfg

Address : 0x44		Register Name : DiagClipOutCfg.SysDiagCfg		Default: 0x0DA50000			
Bits	Access	Default	Field Name	Description			
31:28	Reserved	0x0		Reserved			
27:24		0xD	WatchdogTimeout	Watchdog Timeout 0x0 : 8ms 0x4 : 40ms 0x8 : 100ms 0xC : 1s 0x1 : 10ms 0x5 : 50ms 0x9 : 150ms 0xD : 2s 0x2 : 20ms 0x6 : 60ms 0xA : 200ms 0xE : 4s 0x3 : 30ms 0x7 : 80ms 0xB : 500ms 0xF : 8s			
23:16		0xA5	WatchdogDisableKey	Watchdog Disable Key 0xA5 : Watchdog disabled All other codes enable watchdog			
15:2	Reserved	0x0		Reserved			
1		0x0	ClipOutEn	Two-Sided Clipping to Upper and Lower Diagnostic Limit 0x0 : Disabled 0x1 : Enabled Note: Enabling this feature requires enabling ClipOutEn. Note: DiagOutEn sets the AOUT to either 0% (LDR) or 100% (UDR) Note: UDR will have higher priority than LDR if configuration mixes both failure output signalization states.) Failure signalization of saturation requires enabling of any additional AFE or sensor diagnosis functions.			
0		0x0	DiagOutEn	Output Signalization of Diagnostic State at AOUT 0x0 : Disabled 0x1 : Enabled Note: Clipping limits are defined in DiagClipOutCfg.ClipOutLvl register.			

12.16.2 0x45 – DiagClipOutCfg.DiagOutLvl[0]

Address : 0x45		Register Name : DiagClipOutCfg.DiagOutLvl[0]		Default: 0x00007FFE			
Bits	Access	Default	Field Name	Description			
31:0		0x7FFE	DiagOutLvl[0]	Select register for UDR / LDR assignment of diagnostic checks			

12.16.3 0x46 – DiagClipOutCfg.DiagOutLvl[1]

Address : 0x46		Register Name : DiagClipOutCfg.DiagOutLvl[1]		Default: 0x00000000			
Bits	Access	Default	Field Name	Description			
31:0		0x0	DiagOutLvl[1]	Select register for UDR / LDR assignment of diagnostic checks			

12.16.4 0x47 – DiagClipOutCfg.DiagOutLvl[2]

Address : 0x47		Register Name : DiagClipOutCfg.DiagOutLvl[2]		Default: 0x0000003F			
Bits	Access	Default	Field Name	Description			
31:0		0x3F	DiagOutLvl[2]				

12.16.5 0x48 – DiagClipOutCfg.ClipOutLvl

Address : 0x48		Register Name : DiagClipOutCfg.ClipOutLvl		Default: 0xF3330CCC			
Bits	Access	Default	Field Name	Description			
31:24	Reserved	0xF3		Reserved			
23:16		0x33	ClipOutHigh	Upper Clipping Limit 0xF333 : 95% Full Scale			
15:0		0xCCC	ClipOutLow	Lower Clipping Limit 0x0CCC : 5% Full Scale			

12.16.6 0x49 – CapCtrl

Address : 0x49		Register Name : CapCtrl		Default: 0x00000100
Bits	Access	Default	Field Name	Description
31:12	Reserved	0x0		Reserved
11:8		0x1	SensorAppMode	Capacitive sensor application mode 0x0 : Reserved 0x1 : Application Mode 1 0x2 : Application Mode 2 0x3 : Application Mode 3 0x4 : Application Mode 4 0x5 : Application Mode 5 0x6 : Application Mode 6 0x7 : Application Mode 11
7:5	Reserved	0x0		Reserved
4		0x0	CsInvEnable	Enable 1/C linearization calculation 0x0 : Disabled 0x1 : Enabled
3:2	Reserved	0x0		Reserved
1:0		0x0	ResCapSel	Resistive/Capacitive mode selector 0x0 : Resistive Measurement Only 0x1 : Capacitive Measurement Only

12.16.7 0x4A – CsInvParam

Address : 0x4A		Register Name : CsInvParam		Default: 0x00080000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x80000	RValue	Range-shift value

12.17 SSC Coefficients

12.17.1 0x4D – Bs1Coeff.SOffset

Address : 0x4D		Register Name : Bs1Coeff.SOffset		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	SOffset	Sensor offset term <i>Offset_S</i>

12.17.2 0x4E – Bs1Coeff.SGain

Address : 0x4E		Register Name : Bs1Coeff.SGain		Default: 0x00200000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x200000	SGain	Sensor gain term <i>Gain_S</i>

12.17.3 0x4F – Bs1Coeff.SSot

Address : 0x4F		Register Name : Bs1Coeff.SSot		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	SSot	Second-order term for sensor non-linearity <i>SOT_sens</i>

12.17.4 0x50 – Bs1Coeff.SShift

Address : 0x50		Register Name : Bs1Coeff.SShift		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	SShift	Post-calibration term <i>SENS_shift</i>

12.17.5 0x51 – Bs1Coeff.STco

Address : 0x51		Register Name : Bs1Coeff.STco		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	STco	Temperature coefficient offset term <i>Tco</i>

12.17.6 0x52 – Bs1Coeff.SSotTco

Address : 0x52		Register Name : Bs1Coeff.SSotTco		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	SSotTco	Second-order term for Tco nonlinearity <i>SOT_tco</i>

12.17.7 0x53 – Bs1Coeff.STcg

Address : 0x53		Register Name : Bs1Coeff.STcg		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	STcg	Temperature coefficient gain term <i>Tcg</i>

12.17.8 0x54 – Bs1Coeff.SSotTcg

Address : 0x54		Register Name : Bs1Coeff.SSotTcg		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	SSotTcg	Second-order term for Tcg non-linearity <i>SOT_tcg</i>

12.17.9 0x55 – Bs1Coeff.OutScaleGain

Address : 0x55		Register Name : Bs1Coeff.OutScaleGain		Default: 0x00100000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x100000	OutScaleGain	Post SSC Output Scaling Gain

12.17.10 0x56 – Bs1Coeff.OutScaleOfst

Address : 0x56		Register Name : Bs1Coeff.OutScaleOfst		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	OutScaleOfst	Post SSC Output Scaling Offset

12.17.11 0x57 – Bs2Coeff.SOffset

Address : 0x57		Register Name : Bs2Coeff.SOffset		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	SOffset	Sensor offset term <i>Offset_S</i>

12.17.12 0x58 – Bs2Coeff.SGain

Address : 0x58		Register Name : Bs2Coeff.SGain		Default: 0x00200000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x200000	SGain	Sensor gain term <i>Gain_S</i>

12.17.13 0x59 – Bs2Coeff.SSot

Address : 0x59		Register Name : Bs2Coeff.SSot		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	SSot	Second-order term for sensor non-linearity <i>SOT_sens</i>

12.17.14 0x5A – Bs2Coeff.SShift

Address : 0x5A		Register Name : Bs2Coeff.SShift		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	SShift	Post-calibration term <i>SENS_shift</i>

12.17.15 0x5B – Bs2Coeff.STco

Address : 0x5B		Register Name : Bs2Coeff.STco		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	STco	Temperature coefficient offset term <i>Tco</i>

12.17.16 0x5C – Bs2Coeff.SSotTco

Address : 0x5C		Register Name : Bs2Coeff.SSotTco		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	SSotTco	Second-order term for Tco nonlinearity <i>SOT_tco</i>

12.17.17 0x5D – Bs2Coeff.STcg

Address : 0x5D		Register Name : Bs2Coeff.STcg		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	STcg	Temperature coefficient gain term <i>Tcg</i>

12.17.18 0x5E – Bs2Coeff.SSotTcg

Address : 0x5E		Register Name : Bs2Coeff.SSotTcg		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	SSotTcg	Second-order term for Tcg non-linearity <i>SOT_tcg</i>

12.17.19 0x5F – Bs2Coeff.OutScaleGain

Address : 0x5F		Register Name : Bs2Coeff.OutScaleGain		Default: 0x00100000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x100000	OutScaleGain	Post SSC Output Scaling Gain

12.17.20 0x60 – Bs2Coeff.OutScaleOfst

Address : 0x60		Register Name : Bs2Coeff.OutScaleOfst		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	OutScaleOfst	Post SSC Output Scaling Offset

12.17.21 0x61 – Tch1Coeff.TOffset

Address : 0x61		Register Name : Tch1Coeff.TOffset		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	TOffset	Offset coefficient for temperature <i>Offset_T</i>

12.17.22 0x62 – Tch1Coeff.TGain

Address : 0x62		Register Name : Tch1Coeff.TGain		Default: 0x00200000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x200000	TGain	Gain coefficient for temperature <i>Gain_T</i>

12.17.23 0x63 – Tch1Coeff.TSot

Address : 0x63		Register Name : Tch1Coeff.TSot		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	TSot	Second-order term for temperature source <i>SOT_T</i>

12.17.24 0x64 – Tch1Coeff.TShift

Address : 0x64		Register Name : Tch1Coeff.TShift		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	TShift	Shift for post-calibration/post-assembly offset compensation <i>T_Shift</i>

12.17.25 0x65 – Tch2Coeff.TOffset

Address : 0x65		Register Name : Tch2Coeff.TOffset		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	TOffset	Offset coefficient for temperature <i>Offset_T</i>

12.17.26 0x66 – Tch2Coeff.TGain

Address : 0x66		Register Name : Tch2Coeff.TGain		Default: 0x00200000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x200000	TGain	Gain coefficient for temperature <i>Gain_T</i>

12.17.27 0x67 – Tch2Coeff.TSot

Address : 0x67		Register Name : Tch2Coeff.TSot		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	TSot	Second-order term for temperature source <i>SOT_T</i>

12.17.28 0x68 – Tch2Coeff.TShift

Address : 0x68		Register Name : Tch2Coeff.TShift		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	TShift	Shift for post-calibration/post-assembly offset compensation <i>T_Shift</i>

12.17.29 0x69 – Tch3Coeff.TOffset

Address : 0x69		Register Name : Tch3Coeff.TOffset		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x0	TOffset	Offset coefficient for temperature <i>Offset_T</i>

12.17.30 0x6A – Tch3Coeff.TGain

Address : 0x6A		Register Name : Tch3Coeff.TGain		Default: 0x00200000
Bits	Access	Default	Field Name	Description
31:24	Reserved	0x0		Reserved
23:0		0x200000	TGain	Gain coefficient for temperature <i>Gain_T</i>

12.17.31 0x6B – Tch3Coeff.TSot

Address : 0x6B		Register Name : Tch3Coeff.TSot		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:0		0x0	TSot	Second-order term for temperature source <i>SOT_T</i>

12.17.32 0x6C – Tch3Coeff.TShift

Address : 0x6C		Register Name : Tch3Coeff.TShift		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:0		0x0	TShift	Shift for post-calibration/post-assembly offset compensation <i>T_Shift</i>

12.17.33 0x80 – SscCoeffFmSot.Offset

Address : 0x80		Register Name : SscCoeffFmSot.Offset		Default: 0x40000000
Bits	Access	Default	Field Name	Description
31:0		0x40000000	Offset	

12.17.34 0x81 – SscCoeffFmSot.Gain

Address : 0x81		Register Name : SscCoeffFmSot.Gain		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:0		0x0	Gain	

12.17.35 0x82 – SscCoeffFmSot.Sot

Address : 0x82		Register Name : SscCoeffFmSot.Sot		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:0		0x0	Sot	

12.17.36 0x83 – Afe1MeasCfg5

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x83		Register Name : Afe1MeasCfg5		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31		0x0	AuxMeasEmpty0Aux32	Defines Empty Auxilliary Measurement Task AFE1 0x0 : Disabled 0x1 : Enabled
30		0x0	AuxMeasEmpty0Aux31	
29		0x0	AuxMeasEmpty0Aux30	
28		0x0	AuxMeasEmpty0Aux29	
27		0x0	AuxMeasEmpty0Aux28	
26		0x0	AuxMeasEmpty0Aux27	
25		0x0	AuxMeasEmpty0Aux26	
24		0x0	AuxMeasEmpty0Aux25	
23		0x0	AuxMeasEmpty0Aux24	
22		0x0	AuxMeasEmpty0Aux23	
21		0x0	AuxMeasEmpty0Aux22	
20		0x0	AuxMeasEmpty0Aux21	
19		0x0	AuxMeasEmpty0Aux20	
18		0x0	AuxMeasEmpty0Aux19	
17		0x0	AuxMeasEmpty0Aux18	
16		0x0	AuxMeasEmpty0Aux17	
15		0x0	AuxMeasEmpty0Aux16	
14		0x0	AuxMeasEmpty0Aux15	
13		0x0	AuxMeasEmpty0Aux14	
12		0x0	AuxMeasEmpty0Aux13	
11		0x0	AuxMeasEmpty0Aux12	
10		0x0	AuxMeasEmpty0Aux11	
9		0x0	AuxMeasEmpty0Aux10	
8		0x0	AuxMeasEmpty0Aux9	
7		0x0	AuxMeasEmpty0Aux8	
6		0x0	AuxMeasEmpty0Aux7	
5		0x0	AuxMeasEmpty0Aux6	
4		0x0	AuxMeasEmpty0Aux5	
3		0x0	AuxMeasEmpty0Aux4	
2		0x0	AuxMeasEmpty0Aux3	
1		0x0	AuxMeasEmpty0Aux2	
0		0x0	AuxMeasEmpty0Aux1	

12.17.37 0x84 – Afe1MeasCfg6

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x84		Register Name : Afe1MeasCfg6		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:5	Reserved	0x0		Reserved
4		0x0	AuxMeasEmpty1Aux37	Defines Empty Auxilliary Measurement Task AFE1 0x0 : Disabled 0x1 : Enabled
3		0x0	AuxMeasEmpty1Aux36	
2		0x0	AuxMeasEmpty1Aux35	
1		0x0	AuxMeasEmpty1Aux34	
0		0x0	AuxMeasEmpty1Aux33	

12.17.38 0x85 – Afe2MeasCfg5

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x85		Register Name : Afe2MeasCfg5		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31		0x0	AuxMeasEmpty0Aux32	Defines Empty Auxilliary Measurement Task AFE2 0x0 : Disabled 0x1 : Enabled
30		0x0	AuxMeasEmpty0Aux31	
29		0x0	AuxMeasEmpty0Aux30	
28		0x0	AuxMeasEmpty0Aux29	
27		0x0	AuxMeasEmpty0Aux28	
26		0x0	AuxMeasEmpty0Aux27	
25		0x0	AuxMeasEmpty0Aux26	
24		0x0	AuxMeasEmpty0Aux25	
23		0x0	AuxMeasEmpty0Aux24	
22		0x0	AuxMeasEmpty0Aux23	
21		0x0	AuxMeasEmpty0Aux22	
20		0x0	AuxMeasEmpty0Aux21	
19		0x0	AuxMeasEmpty0Aux20	
18		0x0	AuxMeasEmpty0Aux19	
17		0x0	AuxMeasEmpty0Aux18	
16		0x0	AuxMeasEmpty0Aux17	
15		0x0	AuxMeasEmpty0Aux16	
14		0x0	AuxMeasEmpty0Aux15	
13		0x0	AuxMeasEmpty0Aux14	
12		0x0	AuxMeasEmpty0Aux13	
11		0x0	AuxMeasEmpty0Aux12	
10		0x0	AuxMeasEmpty0Aux11	
9		0x0	AuxMeasEmpty0Aux10	
8		0x0	AuxMeasEmpty0Aux9	
7		0x0	AuxMeasEmpty0Aux8	
6		0x0	AuxMeasEmpty0Aux7	
5		0x0	AuxMeasEmpty0Aux6	
4		0x0	AuxMeasEmpty0Aux5	
3		0x0	AuxMeasEmpty0Aux4	
2		0x0	AuxMeasEmpty0Aux3	
1		0x0	AuxMeasEmpty0Aux2	
0		0x0	AuxMeasEmpty0Aux1	

12.17.39 0x86 – Afe2MeasCfg6

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x86		Register Name : Afe2MeasCfg6		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:5	Reserved	0x0		Reserved
4		0x0	AuxMeasEmpty1Aux37	Defines Empty Auxilliary Measurement Task AFE2 0x0 : Disabled 0x1 : Enabled
3		0x0	AuxMeasEmpty1Aux36	
2		0x0	AuxMeasEmpty1Aux35	
1		0x0	AuxMeasEmpty1Aux34	
0		0x0	AuxMeasEmpty1Aux33	

12.18 Customer ID

12.18.1 0xFD – Customer ID 0

Address : 0xFD		Register Name : Customer_ID_0		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:0		0x0	Customer_ID_0	

12.18.2 0xFE – Customer ID 1

Address : 0xFE		Register Name : Customer_ID_1		Default: 0x00000000
Bits	Access	Default	Field Name	Description
31:0		0x0	Customer_ID_1	

12.19 CCP Version

12.19.1 0xFF – CcpVersion

Address : 0xFF		Register Name : CcpVersion		Default: 0x81020501
Bits	Access	Default	Field Name	Description
31:24		0x81	Pid	
23:16		0x2	PatchVer	CCP Patch Version
15:8		0x5	MinorVer	CCP Minor Version
7:0		0x1	MajorVer	CCP Major Version

13 Application Information

13.1 2-Bridge Application 1.8V to 5.5V Supply

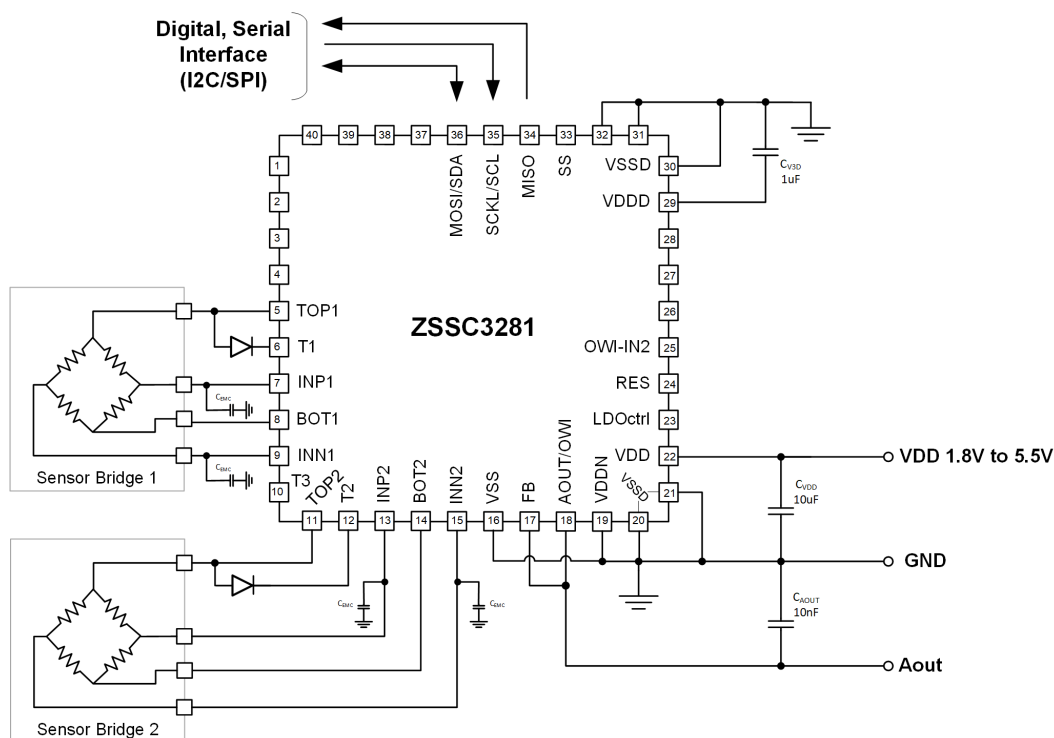


Figure 70: 2-Bridge Application 1.8V to 5.5V Supply

13.2 2-Bridge Application 7V to 48V Supply

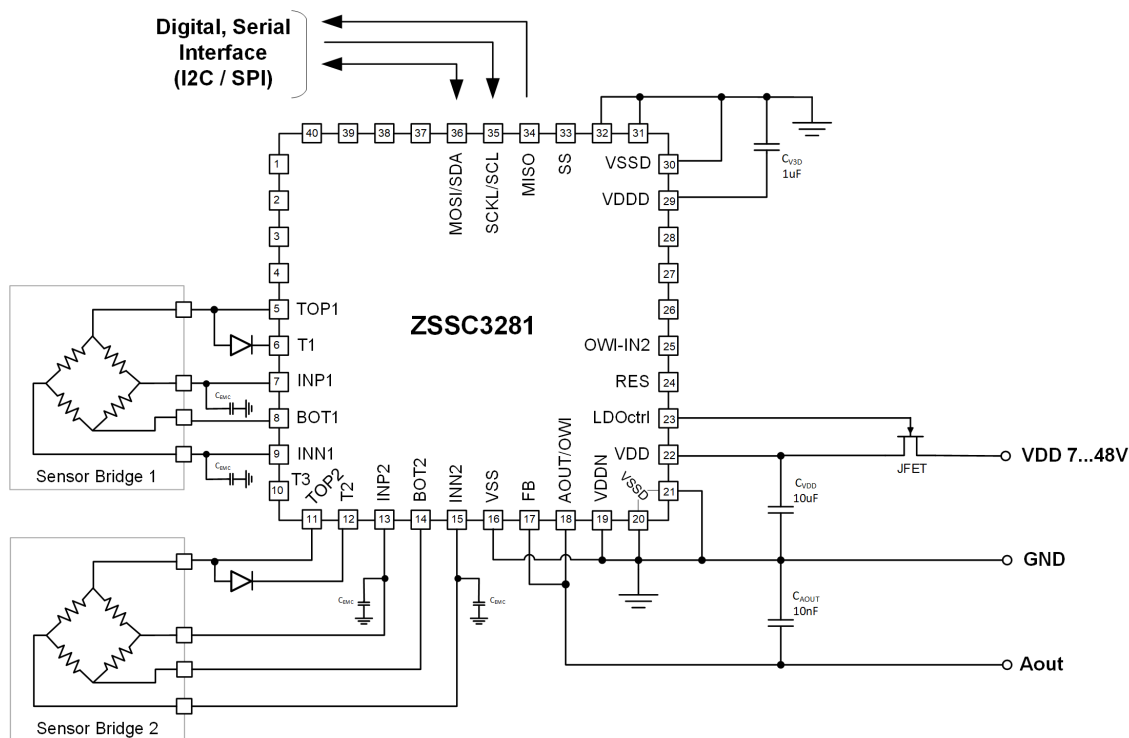


Figure 71: 2-Bridge Application 7V to 48V Supply



13.4 3-Wire Current Loop Application



13.5 Power Supply

13.5.1 Power Supply Modes

ZSSC3281 supports two different main supply modes (Direct VDD Supply and Pre-Regulated High Voltage Supply) and an optional negative voltage supply for the Analog Output Driver. Respective application schematics are shown in 13.5.2 and 13.5.3.

Table 76: Power Supply Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
VDDHV	High voltage supply	Requires external pre-regulator JFET	VDD+0.5		48	V
VDDN	Negative voltage supply for analog output (AOUT)	Internally generated, requires activation of VDDN Charge Pump		$V_{ExtShottky}$		V
		Externally supplied	0	-0.3	-0.5	V
VSS	Analog ground reference			0		V
VSSD	Digital ground reference			0		V
C _{HV}	External high voltage buffer cap	All applications except 2-wire Current Loop		10		μF

13.5.2 Direct VDD Supply

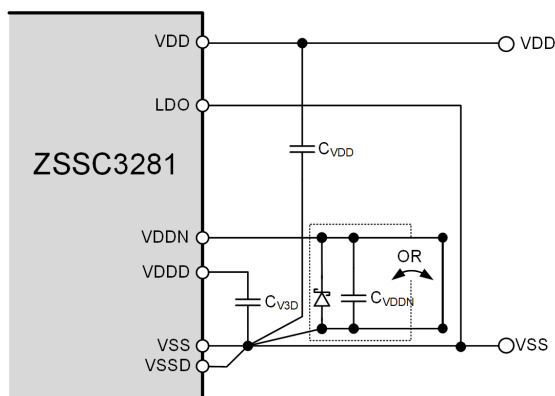


Figure 74: Application with Direct IC Supply

The Direct VDD Supply configuration requires the LDO pin to be connected to VSS on PCB level. To minimize power consumption in all operation modes, the LDO driver circuit is turned off as soon as the user selects 'Direct VDD Supply' mode during device configuration (see GUI Tab: Configure\Power Supply And Oscillator\Supply Mode).

13.5.3 Pre-Regulated High Voltage Supply

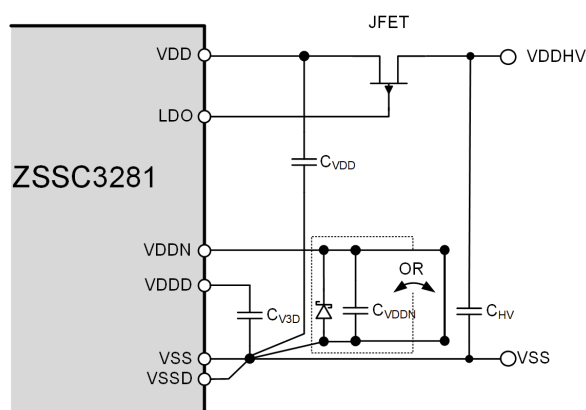


Figure 75: Application with External Regulator

Higher than 5.25V supply voltages require an external JFET as pre-regulation device. The LDO output pin of ZSSC3281 is able to drive the JFET devices listed in Table 77 in a circuit configuration as shown in Figure 75.

Table 77: Supported JFET Devices

Manufacturer	Type	Typical $V_{GS(TH)}$	Typical ID/A at 25°C
Supertex inc.	DN3545	-3.5V to -1.5V	0.2
Infineon	BSP149	-1.8V to -1V	0.66
Infineon	BSS169	-2.9V to -1.8V	0.17

The output voltage of the JFET assisted pre-regulator is configurable as shown in Table 78. In the GUI it can be configured through the field Configure\Power Supply And Oscillator\Regulated VDD.

Table 78: Configurable Pre-Regulator

Output Voltage (VDD)	VDDHV Min	VDDHV Max ¹	Unit
3	3.5	48	V
4	4.5	48	V
5	5.5	48	V
5.25	5.75	48	V

¹ VDDHV depends on selected external JFET parameters.

Besides the VDD buffer capacitor C_{VDD} another buffer capacitor C_{HV} is recommended on the high voltage supply VDDHV for stability reasons.

13.5.4 Negative Voltage Supply for AOUT

To support True-0V signals on the Analog Output (AOUT), ZSSC3281 provides an option to externally supply a negative voltage rail for the AOUT buffer at VDDN. VDDN supply specifications are shown in 76.

The negative VDDN voltage can also be generated by an internal charge pump circuit. The internal charge pump can be activated through GUI field: Configure\AOUT\VDDN Charge Pump.

The charge pump function is only available for all AOUT Operation Modes with Voltage Output. The charge pump circuit requires an external buffer capacitor C_{VDDN} and a Schottky Diode to work properly.

If no True-0V signals are required at AOUT, the user must directly connect VDDN with VSS on PCB level.

14 Package Information

14.1 Package Outline Drawings

The package outline drawings are accessible from the link below. The package information is the most current data available.

QFN40: [Package Outline Drawing Code: NDG40S1 40-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.4 mm Pitch \(renesas.com\)](#)

WLCSP: [Package Outline Drawing Code: AWG48D1 48-DSBGA 3.61 x 3.24 x 0.6 mm Body, 0.4 mm Pitch \(renesas.com\)](#)

14.2 QFN40 Marking Diagram

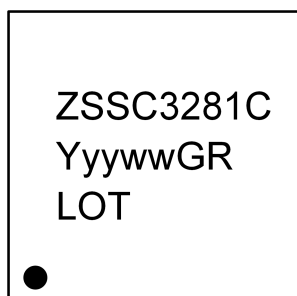


Figure 76: QFN40 Marking Diagram

1. "ZSSC3281" C is the truncated part number.
2. "YyywwGR" where "Y" and "GR" are fixed and "yyww" represents the last digits of the year and week that the part was assembled.
3. "LOT" is the complete lot number of the part.

14.3 WLCSP Marking Diagram

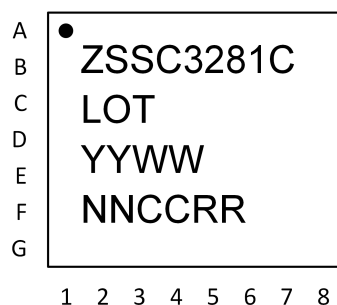


Figure 77: WLCSP Marking Diagram

1. "ZSSC3281C" is the truncated part number.
2. "LOT" is the complete lot number of the part.
3. "YYWW" represents the last digits of the year and week that the part was assembled.
4. "NNCCRR" contains the wafer position information:
 - "NN": Scribe Number
 - "CC": Column of die location
 - "RR": Row of die location

15 Glossary, References and History

15.1 Glossary

Term	Description
ADC	Analog to Digital Converter
AFE	Analog Front End
ARM	Provider of microcontroller core
AUX	Auxiliary measurement, in addition to main sensor bridge measurement
AZ	Auto-zero
BLOB	Binary Large Object
BOT	Bottom
CCP	Configuration and Calibration Page
CVC	Capacitance to Voltage Converter
DAC	Digital to Analog Converter
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FB	Feedback input for analog output buffer
FS	Full Scale
FW	Firmware
GPIO	General Purpose Input Output
GUI	Graphical User Interface
HF	High Frequency
HW	Hardware
I2C	Inter Integrated Circuit communication protocol
ID	Identification
IIR	Infinite Impulse Response
ISDU	Indexed Service Data Unit
LDR	Lower Diagnostic Range
LF	Low Frequency
LSB	Least Significant Bit
MISO	Master-In Slave-Out
MOSI	Master-Out Slave-In
MSB	Most Significant Bit
OWI	One Wire Interface
PGA	Programmable Gain Amplifier
PHY	Physical Layer
POR	Power-On-Reset
PTAT	Proportional to absolute temperature current source
R	Read
RAM	Random Access Memory
RCA	Renesas Code Area
RDAC	Resistive Digital to Analog Converter
RTD	Temperature dependent resistor
RW	Read/Write
SM-	Main Sensor Measurement, inverted signal polarity
SM+	Main Sensor Measurement, standard (non-inverted) signal polarity
SOT	Second Order Term
SPI	Serial Peripheral Interface
SS	Slave Select
SSC	Sensor Signal Conditioner

Continued on next page

Term	Description
SSP	Smart Sensor Profile
TFW	Technology Firmware
TLC	Third Logic Channel
UART	Universal Asynchronous Receiver / Transmitter
UDR	Upper Diagnostic Range
W	Write
WURQ	Wake-Up Request

15.2 Firmware Revision History

Revision	Date	Description
1.6.0	November 27, 2025	Capacitive Front End enabled New Meas Commands
1.5.0	January 31, 2025	Initial release revision C
1.4.0	November, 2023	Latest release for revision B

15.3 Document Revision History

Revision	Date	Description
2.1	December 8, 2025	Capacitive Front End added I2C CRC and PinSelection added New Meas Commands added
2.0	July 7, 2025	Initial release revision C
1.3	March 13, 2023	Latest release for revision B